PanaXSeries

The One to Watch for Constant Innovation-Making the Future Come Alive

MICROCOMPUTER MN1500

MN150222/P0222

LSI User's Manual

Pub.No.20122-030E

Panasonic

PanaXSeries is a trademark of Matsushita Electric Industrial Co., Ltd.

The other corporation names,logotype and product names written in this book are trademarks or registered trademarks of their corresponding corporations.

Request for your special attention and precautions in using the technical information and semiconductors described in this book

(1) An export permit needs to be obtained from the competent authorities of the Japanese Government if any of the products or technologies described in this book and controlled under the "Foreign Exchange and Foreign Trade Law" is to be exported or taken out of Japan.

(2) The contents of this book are subject to change without notice in matters of improved function. When finalizing your design,therefore,ask for the most up-to-date version in advance in order to check for any changes.

(3) We are not liable for any damage arising out of the use of the contents of this book, or for any infringement of patents or any other rights owned by a third party.

(4) No part of this book may be reprinted or reproduced by any means without written permission from our company.

(5) This book deals with standard specifications. Ask for the latest individual Product Standards or Specifications in advance for more detailed information required for your design,purchasing and applications.

If you have any inquiries or questions about this book or our semiconductors, please contact one of our sales offices listed at the back of this book or Matsushita Electronics Corporation's Sales Department.

Contents

CHAPTER 1 OVERVIEW
- 1.1 Overview
- 1.2 Features
- 1.3 Pin Assignment
- 1.4 Pin Descriptions
- 1.5 Unused Pins
- 1.6 Block Diagram
- 1.7 Electrical Characteristics
- 1.8 Package

CHAPTER 2 CPU CORE FUNCTIONS
- 2.1 Clock Generator and CPU Basic Timing
- 2.2 ROM and RAM
- 2.3 Stack Area
- 2.4 Flag Status
- 2.5 Backup Mode
- 2.6 Reset
- 2.7 Clock Switching Function

CHAPTER 3 I/O REGISTER FUNCTIONS
- 3.1 I/O Registers List
- 3.2 Allocation and Description of Registers
- 3.3 Available Instructions
- 3.4 Pin Structure Diagram

CHAPTER 4 INTERRUPT FUNCTIONS
- 4.1 Interrupt Control
- 4.2 Interrupt Receiving Operation
- 4.3 Interrupt Return Operation
- 4.4 Stack upon Interrupt

CHAPTER 5 TIMER FUNCTION

CHAPTER 6 TIME BASE FUNCTION

CHAPTER 7 A/D CONVERSION FUNCTION

CHAPTER 8 AC ZERO VOLTAGE DETECTION FUNCTION

CHAPTER 9 WATCHDOG TIMER FUNCTION

CHAPTER 10 INSTRUCTION SETS

CHAPTER 11 PRODUCT WITH ON-CHIP EPROM

* This document is based on an equivalent Japanese document that was revised on Dec. 1999.

CHAPTER 1 OVERVIEW

1.1 Overview

This is a high-performance, low power-consuming, 4-bit, single-chip CMOS microcomputer LSI with each 2-Kbyte ROM and 96-nibble RAM.
For peripheral devices, the LSI incorporates a 10-bit A/D converter, AC zero voltage detection circuit, each 8-bit timer/counter, time base block, LED direct drive pin, Hi-Z output port control circuit, auto reset circuit and watchdog timer. The auto reset circuit and watchdog timer are mask optional functions.

1.2 Features

[Hardware Features]

ROM capacity : 2048 × 8 bits
RAM capacity : 96 × 4 bits
Instruction execution frequency: 1/8 f_{osc}
Machine cycle : 1.00 µs 1/8 × 8.00 MHz
V_{DD}=4.5 V to 5.5V
4.00 µs 1/8 × 2.00 MHz
V_{DD}=2.0 V to 5.5 V without auto reset circuit
(V_{DD}=V_{RSTL1} to 5.5 V with auto reset circuit)
8.00 µs 1/8 × 1.00 MHz
V_{DD}=1.8 V to 5.5 V without auto reset circuit
(V_{DD}=V_{RSTL1} or V_{RSTL2} to 5.5 V with auto reset circuit)
Interrupt : 1 level
(Software is selected with timer, time base, external interrupt or AC zero voltage detection interrupt.)
Backup mode : STOP/HALT mode
Timer/Counter : Timer/Event count function
Time base : Time base and buzzer outputs function
Watchdog timer : Resettable in approx. 33-ms cycle (at f_{osc}=8.00 MHz) (Mask option)
A/D converter : Max. 4-channel A/D conversion input, dividing into 1024 between V_{DD} and V_{SS} voltages
AC zero voltage detection circuit: ACZ pin (shared with P31/$\overline{IRQ}$)
LED direct drive pin : 7 V (breakdown voltage) ×4 pins
Auto reset circuit : V_{RSTL1} can be used when one machine cycle is 4 ms or more.
V_{RSTL2} can be used when one machine cycle is 8 ms or more.
(Mask option)
I/O pins Hi-Z control : (Software selection)
Pull-up resistor setting : (Mask option)
I/O pin output type : (Push-pull or N-ch open-drain type) (Mask option)

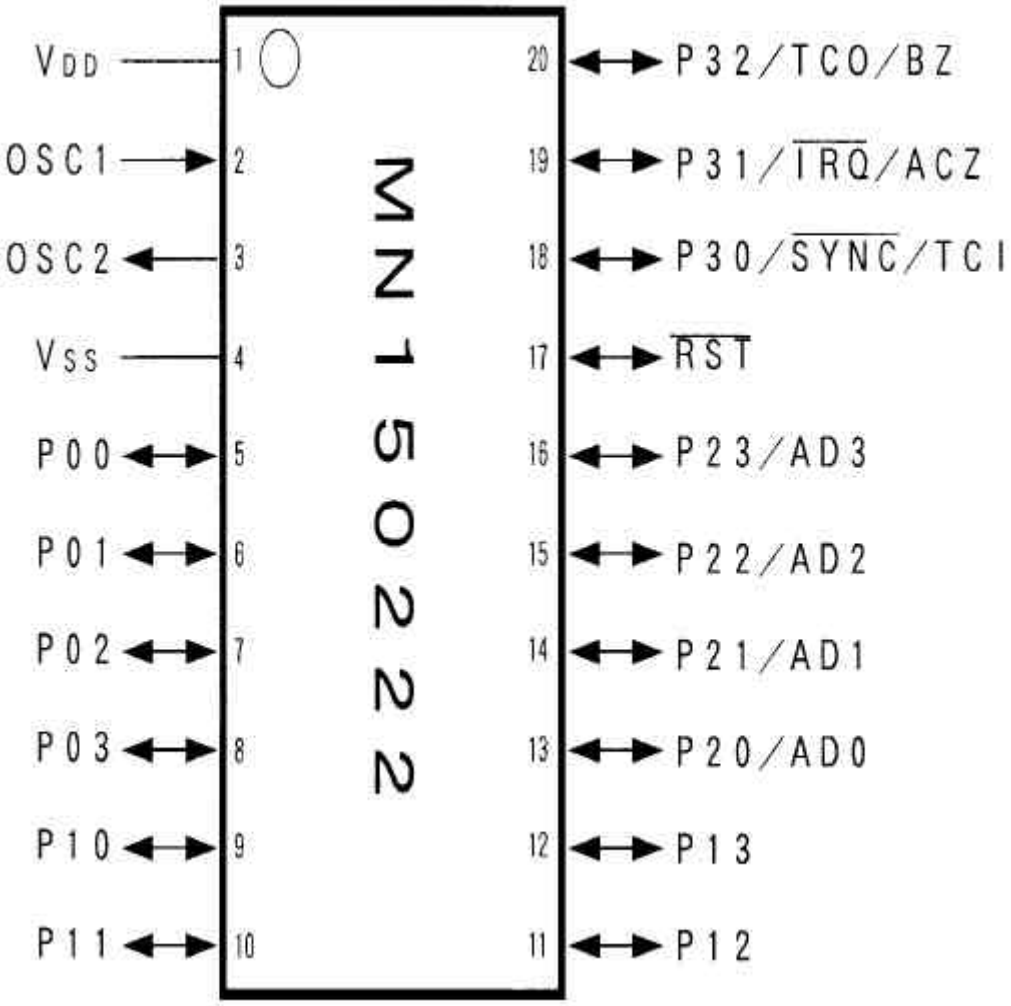
I/O pins:	General-purpose I/O pins	15 pins
	A/D converter input	Max. 4 pins (used in common with general-purpose I/O)
	Timer output/Buzzer output	1 pin (used in common with general-purpose I/O)
	IRQ/ACZ input	1 pin (used in common with general-purpose I/O)
	LED direct drive output	4 pins (N-ch open-drain output) (used in common with general-purpose input)
	$\overline{SYNC}$ pin/Timer input	1 pin (used in common with general-purpose I/O)
	Oscillator pin	2 pins

Package : 20-pin SOP, 22-pin SDIP
Process : Silicon gate CMOS

[Software Features]

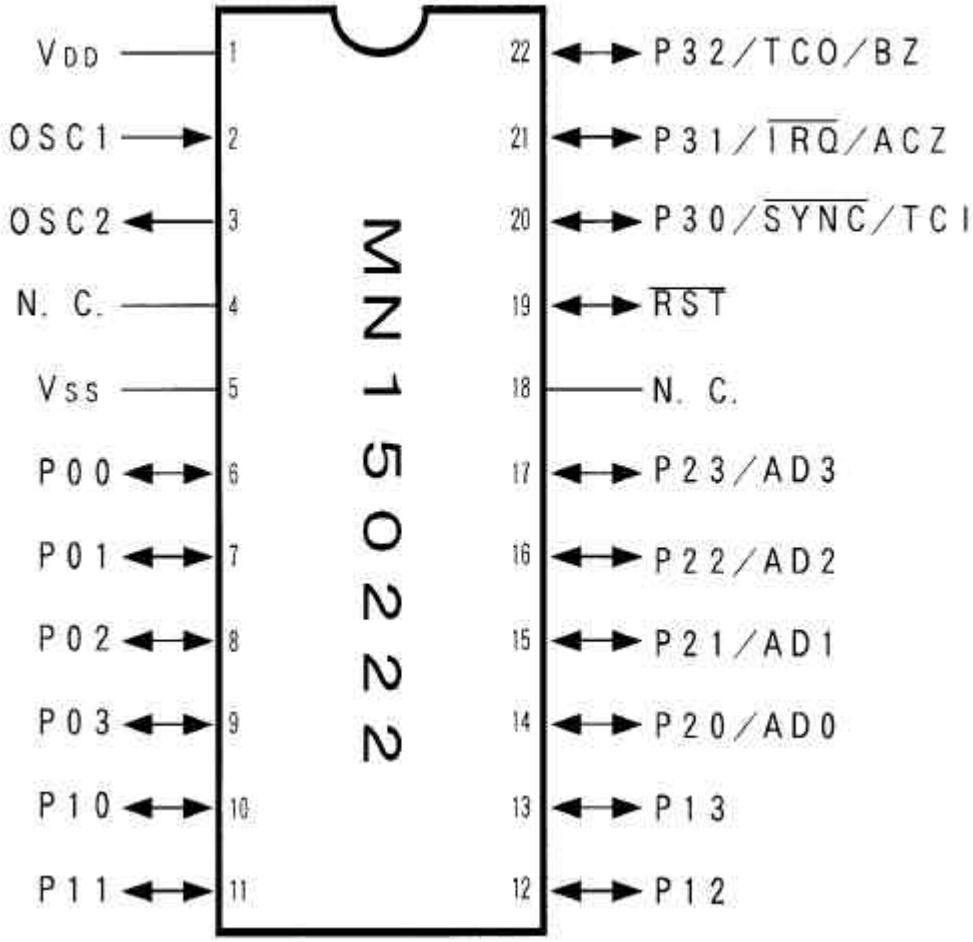
- Total 51 instructions
- Direct addressing computation for all RAM areas
- Non-page program counter
- 4-/1-bit operational instructions

1.3 Pin Assignment



20-PIN SOP TOP VIEW

MN150222 Pin Assignment 1



Note) No device is connected to the N.C. pin.

22-PIN SDIP TOP VIEW

MN150222 Pin Assignment 2

1.4 Pin Descriptions

Symbol	Name	I/O	Function	Initial State
V_{DD} V_{SS}	Power supply pins	——	Apply +1.8 V to +5.5 V to V_{DD}, and 0 V to V_{SS}.	——
OSC1 OSC2	Clock input Clock output	I O	Oscillator connection pins. A feedback resistor is built in.	——
$\overline{RST}$	Reset input	I/O	The LSI is reset with low-level input into this pin. In order to reset the LSI without fail,it is recommendable to turn on low-level input into this pin for one machine cycle or more. The pin incorporates a Schmitt input circuit. The pull-up resistor connection is specified according to the mask option. Whenever reset input is cleared, the LSI waits for a certain period for the stabilization of oscillation. After that, the internal reset status of the LSI is cleared. This pin is used as an output pin of the mask optional auto reset circuit and watchdog timer circuit as well.	——
P00 to P03	Parallel data I/O	I/O	4-bit parallel data I/O ports. Output type is N-ch open-drain. Capable of directly driving the LED.	Port input
P10 to P13	Parallel data I/O	I/O	4-bit parallel data I/O ports. Output type of N-ch open-drain or push-pull and a pull-up resistor connection can be specified by mask option.	Port input
P20/AD0 to P23/AD3	Parallel data I/O (A/D converter input)	I/O (I)	4-bit parallel data I/O ports. Output type of N-ch open-drain or push-pull and a pull-up resistor connection can be specified by mask option. Each of these pins is switched in single-bit increments with software so that these pins will be available to A/D conversion input for a maximum of four channels.	Port input

Symbol	Name	I/O	Function	Initial State
P30 /SYNC /TCI	Parallel data I/O (Sync signal output) (Timer input)	I/O (O) (I)	Parallel data I/O port. Output type of N-ch open-drain or push-pull and a pull-up resistor connection can be specified by mask option. The SYNC internal timing signal is output from this pin when the LSI is reset or within two machine cycles after the internal reset status of the LSI is cleared. The pin has push-pull output regardless of mask optional specifications while the SYNC timing signal is output. The TCI timer input pin incorporates a Schmitt input circuit. If the clock source of the timer is set to the TCI input with software, the output of P30/SYNC/TCI will be Hi-Z state.	CPU timing output at reset Port input after clearing reset
P31 /IRQ /ACZ	Parallel data I/O (External interrupt) (AC zero voltage input)	I/O (I) (I)	Parallel data I/O port. The IRQ external interrupt pin incorporates a Schmitt input circuit. Output type of N-ch open-drain or push-pull and a pull-up resistor connection can be specified by mask option. The output of P31/IRQ/ACZ pin will be Hi-Z state if the external interrupt function or AC zero voltage detection interrupt function is selected with software.	Port input
P32 /TCO /BZ	Parallel data I/O (Timer output) (Buzzer output)	I/O (O) (O)	Parallel data I/O port. Output type of N-ch open-drain or push-pull and a pull-up resistor connection can be specified by mask option. This pin is switched over with software so that timer or buzzer output from this pin will be enabled.	Port input

Note) The port input as an initial status described in the above table is applicable while the LSI is under Hi-Z control. After the Hi-Z status is cleared, each pin has output according to the mask option.

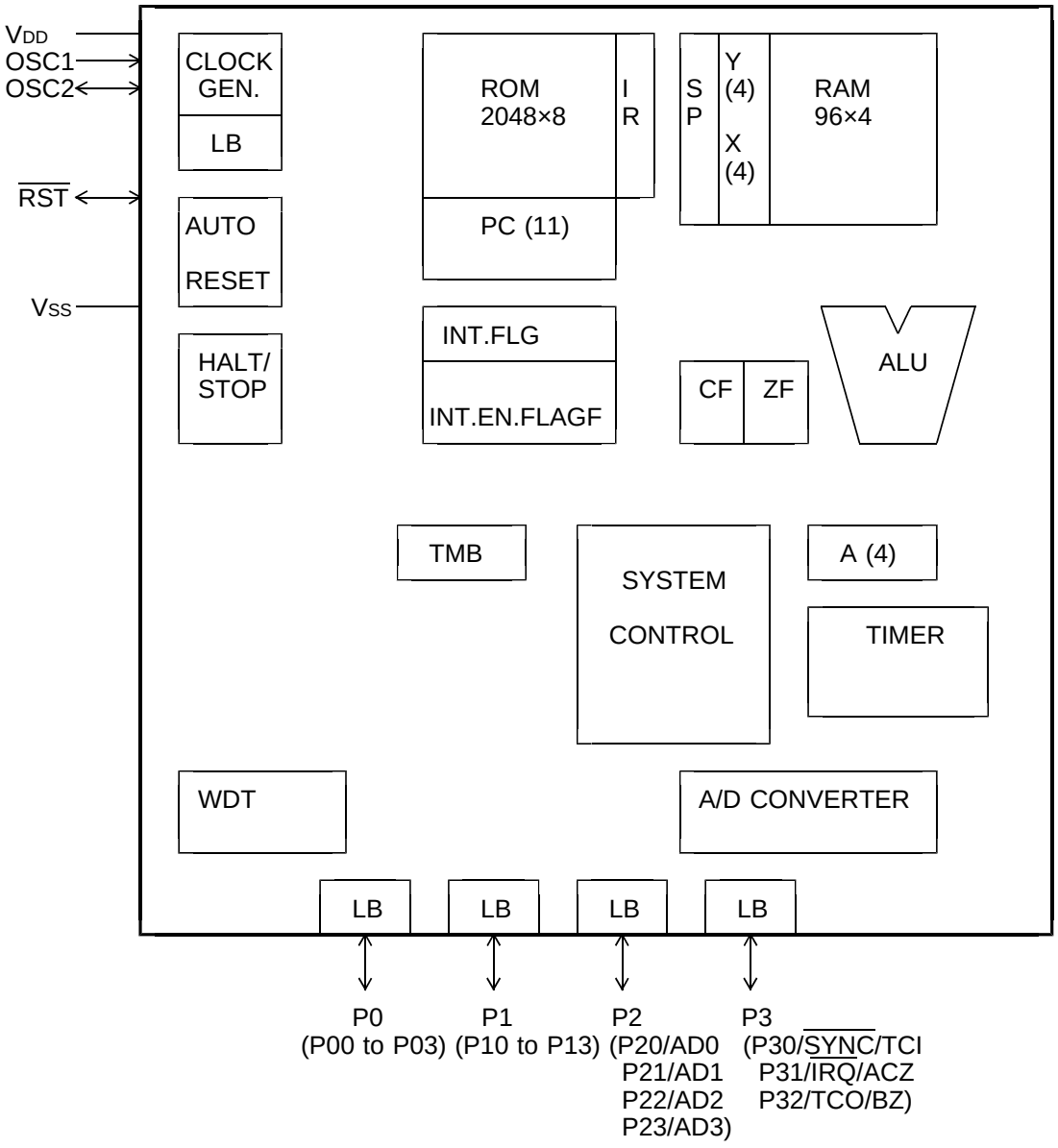
1.5 Unused Pins

It is recommendable to fix each unused pin to the status shown in the following table.

Pin name	Output type	Pull-up resistor	Fixation method
P00 to P03	N-ch open-drain	Selection disabled	Fixed to "L"
P10 to P13	N-ch open-drain N-ch open-drain	ON OFF	Open Fixed to "L"
P20/AD0 to P23/AD3 I/O port selection	N-ch open-drain N-ch open-drain	ON OFF	Open Fixed to "L"
P30/$\overline{\text{SYNC}}$/TCI	N-ch open-drain N-ch open-drain	ON OFF	Open Fixed to "L" via a 1-kW resistor
P31/$\overline{\text{IRQ}}$/ACZ I/O port selection	N-ch open-drain N-ch open-drain	ON OFF	Open Fixed to "L"
P32/TCO/BZ I/O port selection	N-ch open-drain N-ch open-drain	ON OFF	Open Fixed to "L"
P10 to P13, P20 to P23P30 to P32 I/O port selection	CMOS push-pull	Selection disabled (OFF)	Open

Make the above settings, provided that the LSI is not under Hi-Z control.

1.6 Block Diagram



Description of Block Diagram

Block		Function
Instruction Execution Control Block	IR	An instruction, which the CPU is about to execute, is read from the ROM and latched into the instruction register.
	ROM	The read only memory (ROM) is a program memory and stores a program to be run.
Register Block	PC	The program counter is a 11-bit register which controls the execution sequence of the instructions in the program memory. See Note.
	SP	The stack pointer (SP) is a 4-bit register indicating the address of the stack area which uses a part of the data RAM. The stack area is used to save the PC, etc. when a subroutine call or interrupt occurs.
	X	X is a 4-bit register for indirect addressing of the RAM space.
	Y	Y is a 4-bit register for indirect addressing of the RAM space.
Arithmetic Block	ALU	The arithmetic and logic unit (ALU) performs arithmetic operations (addition, subtraction, increment, decrement and comparison) and logical operations (AND, OR, XOR, complement and rotate).
Flag Block	FS (CF) (ZF)	The flag status (FS) consists of two kinds of flags which indicate the running condition of the CPU. The carry flag (CF) is set when an ALU operation result either overflows or underflows. The zero flag (ZF) is set when an ALU operation result is zero, or otherwise, reset.
Data Memory Block	RAM	The random access memory (RAM) is used both as a stack area and a data area which accumulates the data required for running the program.
Interrupt Control Block	IF IE	This block controls an interrupt using the interrupt control flag (IF) and interrupt enable flag (IE).
Timer/Counter Block	TM TB BC	The timer/counter consists of TM which sets either the timer or event count mode and frequency dividing ratio, TB which sets a timer value and BC, a binary counter, which counts pulses.
Time Base Block	TMB	The time base block divides the frequency of the clock signal f_{osc} by the frequency dividing ratio selected with software.

Note) Set the bits of the program counter as indicated below.

(MSB)			(LSB)
10 9 8	7 6 5 4	3 2 1 0	
PCh	PCm	PCl	

Block		Function
Oscillation Block	CLOCK GENE-RATOR	Connect a system clock oscillator between OSC1 and OSC2.
Auto Reset	AUTO RESET	The auto reset function enables the low-voltage detection circuit to operate and sets the $\overline{RST}$ pin to low level when the V_{DD} drops to or below V_{RSTL} voltage.
Watchdog Timer	WDT	The clock of $f_{osc}/2^{12}$ is divided by 2^6 through the watchdog timer. The watchdog timer outputs a low-level signal to the $\overline{RST}$ pin if an overflow occurs.
A/D Converter	A/D CON-VERTER	The A/D converter has a resolution of 10 bits with a maximum of four analog input channels. The analog input between the V_{DD} and V_{SS} voltages are divided by 1024 to convert the analog input into digital values.
Others	V_{SS} V_{DD} $\overline{RST}$	V_{SS} and V_{DD} are power supply pins. Apply +1.8 V to +5.5 V to V_{DD}. $\overline{RST}$ is a reset pin and activated when the $\overline{RST}$ pin is at high level.

1.7 Electrical Characteristics (See Note 1.)

Type	MOS LSI
Function	CMOS 4-bit single-chip microcomputer

A. Absolute Maximum Ratings Ta = 25 °C V_{SS} = 0 V

	Parameter	Symbol	Rating	Unit
A1	Supply voltage	V_{DD}	-0.3 to +7.0	V
A2	Input clamp current (P31/IRQ/ACZ)	I_C	-0.5 to +0.5	mA
A3	Input pin voltage	V_I	-0.3 to V_{DD} +0.3 * Not applicable to P31/$\overline{IRQ}$/ACZ	V
A4	Output pin voltage	V_O	-0.3 to V_{DD} +0.3	V
A5	High-current output pin voltage	V_{OH}	-0.3 to +7.0	V
A6	I/O pin voltage	V_{IO}	-0.3 to V_{DD} +0.3	V
A7	Peak output current (Other than P0)	$I_{OH(Peak)}$ $I_{OL(Peak)}$	-10 20	mA
A8	Peak output current (P0)	$I_{OL(Peak)}$	40	mA
A9	Average output current (See Note 2.) (Other than P0)	$I_{OH(avg)}$ $I_{OL(avg)}$	-2 10	mA
A10	Average output current (See Note 2.) (P0)	$I_{OL(avg)}$	15	mA
A11	Power dissipation	P_D	See Note 3.	mW
A12	Operating ambient temperature	T_{opr}	-40 to +85	°C
A13	Storage temperature	T_{stg}	-55 to +125	°C

Note 1) Those electrical characteristics are reference values. For details, refer to the Product Standards.
Note 2) Applied to any 100 ms period.
Make sure that the total output current value of all output pins is 30 mA or less for 20-pin SOP and 50 mA or less for 22-pin SDIP.
Note 3) 22-pin SDIP: P_D = 350 mW
20-pin SOP : P_D = 180 mW

B. Operating Conditions

Ta = -40 °C to +85 °C, V_{DD} = 1.8 V to 5.5 V (V_{RSTL1} or V_{RSTL2} to 5.5 V), V_{SS} = 0 V

See Note.

Parameter		Symbol	Conditions	Limits			Unit
				min	typ	max	
B1	Supply voltage	V_{DD1}	Machine cycle: 1.0 µs High-speed oscillation mode	4.5	5.0	5.5	V
		V_{DD2}	Machine cycle: 4.0 µs High-speed oscillation mode without auto reset	2.0		5.5	
		V_{DD3}	Machine cycle: 8.0 µs High-speed oscillation mode without auto reset	1.8		5.5	
		V_{DD4}	Machine cycle: 64.0 µs Low-speed oscillation mode without auto reset	1.8		5.5	
		V_{DD5}	Machine cycle: 4.0 µs or more High-/low-speed oscillation modes with auto reset	V_{RSTL1}		5.5	
		V_{DD6}	Machine cycle: 8.0 µs or more High-/low-speed oscillation modes with auto reset	V_{RSTL1} V_{RSTL2}		5.5	

Note) V_{RSTL1} and V_{RSTL2} voltages refer to the supply voltages that are detected to reset the LSI, which are applicable if the auto reset circuit is selected as a mask option.

Auto Reset Circuit 1

B2	Voltage detection level	V_{RSTH1}	Fig. 1		3.1	4.0	V
		V_{RSTL1}		2.0	3.0		
B3	Hysteresis width	V_H		0.05	0.1		
B4	Supply voltage change rate	$\Delta t/\Delta V$		1.00			ms/V

* The above values are applied when use of the auto reset function is selected as a mask option and the LSI is operated by the normal 5-V supply voltage.

Auto Reset Circuit 2

B5	Voltage detection level	V_{RSTH2}	Fig. 1		2.0	2.6	V
		V_{RSTL2}		1.2	1.9		
B6	Hysteresis width	V_H		0.05	0.1		
B7	Supply voltage change rate	$\Delta t/\Delta V$		1.00			ms/V

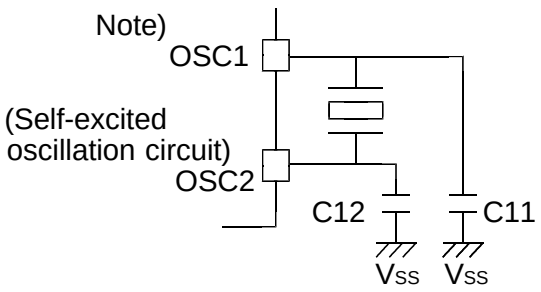
* The above values are applied when use of the auto reset function is selected as a mask option and the LSI is operated by the normal 3-V supply voltage.

Operating Speed Ta= -40 °C to +85 °C, V_{DD}=1.8 V to 5.5 V (V_{RSTL1} or V_{RSTL2} to 5.5V), V_{SS}=0 V

Parameter		Symbol	Conditions	Limits			Unit
				min	typ	max	
B8	Instruction execution time	t_{c1}	V_{DD}=4.5 V to 5.5 V High-speed oscillation mode f_{osc}=8.0 MHz		1.0		µs
		t_{c2}	V_{DD}=2.0 V (V_{RSTL1}) to 5.5 V High-speed oscillation mode f_{osc}=2.0 MHz ( ): At auto reset ON		4.0		
		t_{c3}	V_{DD}=1.8 V(V_{RSTL1} or V_{RSTL2}) to 5.5 V High-speed oscillation mode f_{osc}=1.0 MHz ( ): At auto reset ON		8.0		
		t_{c4}	V_{DD}=1.8 V (V_{RSTL1} or V_{RSTL2}) to 5.5 V Low-speed oscillation mode f_{osc}=125 kHz ( ): At auto reset ON		64.0		

Oscillation OSC1, OSC2 (See Note.)

B9	Oscillator frequency	f_{Xtal1}	V_{DD}=1.8 V to 5.5 V High-speed oscillation mode	0.5		8.0	MHz
		f_{Xtal2}	V_{DD}=1.8 V to 5.5 V Low-speed oscillation mode	32		125	kHz



- Have the sample of the above circuits evaluated by oscillator manufacturer to determine the external capacitance each of C11 and C12. In most cases, the appropriate value of each capacitor seems to be approx. 30 pF.
- The LSI has an on-chip feedback resistor.

External Clock Input 1 OSC1 (High-speed oscillation mode. OSC2 is open.)
Ta= -40 °C to +85 °C, V_{DD}=1.8 V to 5.5 V (V_{RSTL1} or V_{RSTL2} to 5.5 V), V_{SS}=0 V

Parameter		Symbol	Conditions	Limits			Unit
				min	typ	max	
B10	Clock frequency	f_{osc1}		1.0		8.0	MHz
	High-level pulse width *	t_{wh1}	Fig. 2 A clock duty ratio should be 45 % to 55 %.	40			ns
	Low-level pulse width *	t_{wl1}		40			
	Rise time	t_{wr1}	Fig. 2			20	
	Fall time	t_{wf1}				20	
	Input voltage high level	V_{IH1}		0.8V_{DD}		V_{DD}	V
	Input voltage low level	V_{IL1}		V_{SS}		0.2V_{DD}	

External Clock Input 2 OSC1 (Low-speed oscillation mode. OSC2 is open.)

B11	Clock frequency	f_{osc2}		32		125	MHz
	High-level pulse width *	t_{wh2}	Fig. 3 A clock duty ratio should be 45 % to 55 %.	0.8			ns
	Low-level pulse width *	t_{wl2}		0.8			
	Rise time	t_{wr2}	Fig. 3			20	
	Fall time	t_{wf2}				20	
	Input voltage high level	V_{IH2}		0.8V_{DD}		V_{DD}	V
	Input voltage low level	V_{IL2}		V_{SS}		0.2V_{DD}	

External Clock Input 3 TCI

Ta= -40 °C to +85 °C, V_{DD}=1.8 V to 5.5 V (V_{RSTL1} or V_{RSTL2} to 5.5 V), V_{SS}=0 V

Parameter		Symbol	Conditions	Limits			Unit
				min	typ	max	
B12	Clock frequency	f_{tci}	V_{DD} = 1.8 V to 5.5 V Fig. 4			5	MHz
	High-level pulse width *	t_{wh3}		100			ns
	Low-level pulse width *	t_{wl3}		100			
	Clock frequency	f_{tci}	V_{DD} = V_{RSTL} to 1.8 V Fig. 4			2.5	MHz
	High-level pulse width *	t_{wh3}		200			ns
	Low-level pulse width *	t_{wl3}		200			
	Rise time	t_{rcp}	Fig. 4			20	
	Fall time	t_{fcp}				20	
	Input voltage high level	V_{IH3}		0.8V_{DD}		V_{DD}	V
	Input voltage low level	V_{IL3}		V_{SS}		0.1V_{DD}	

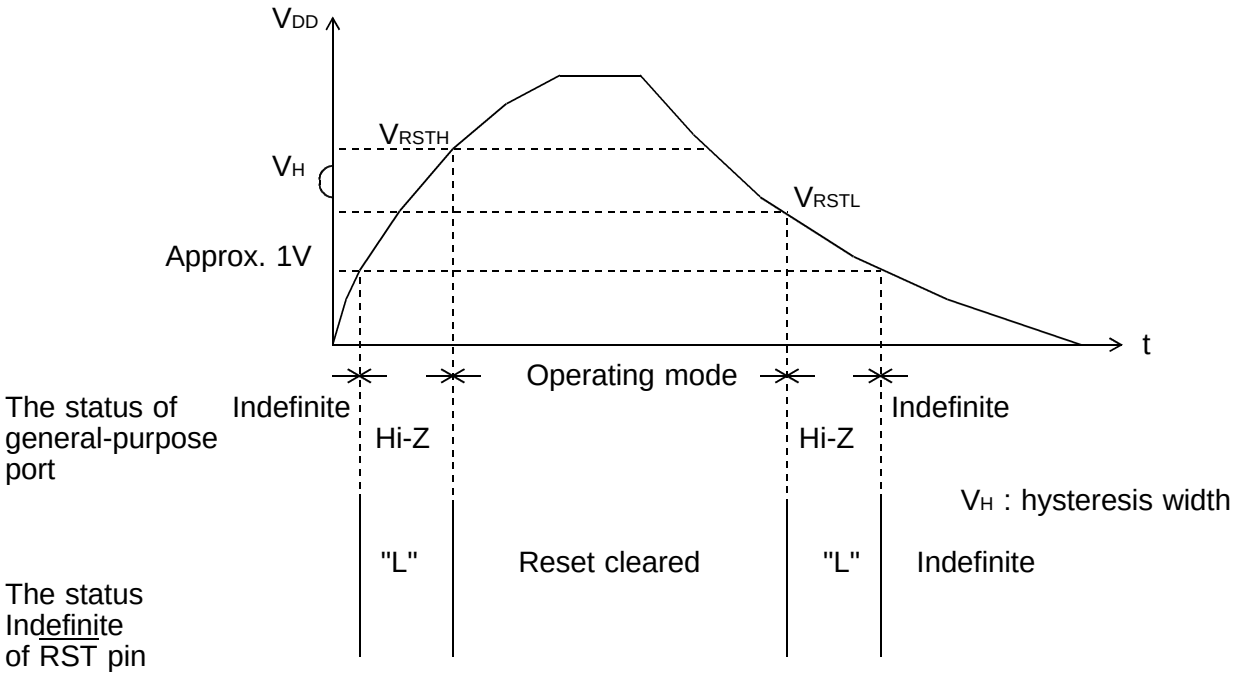


Fig. 1 Auto Reset Voltage

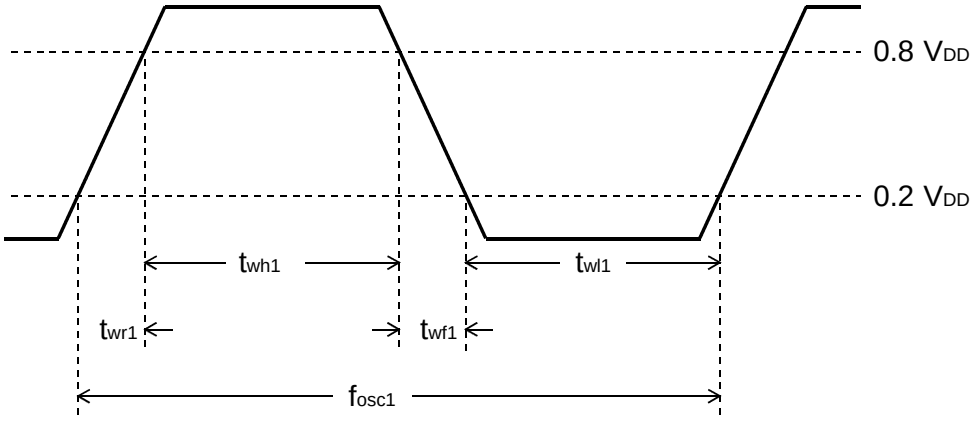


Fig. 2 OSC1 Timing Chart

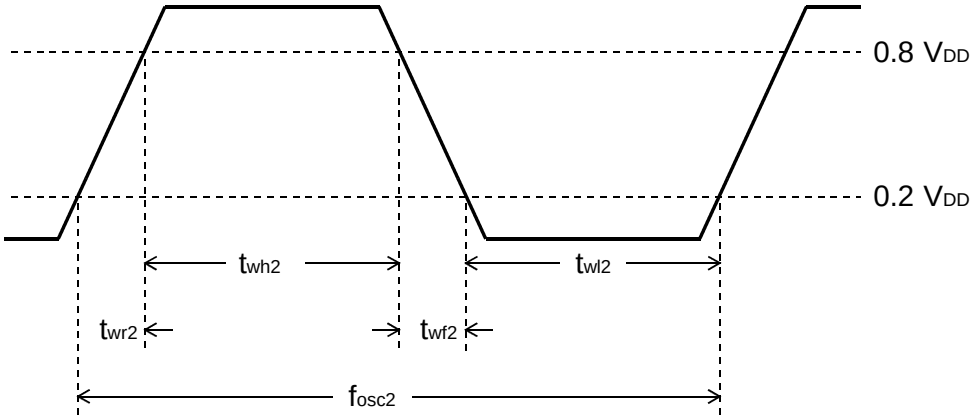


Fig. 3 OSC1 Timing Chart

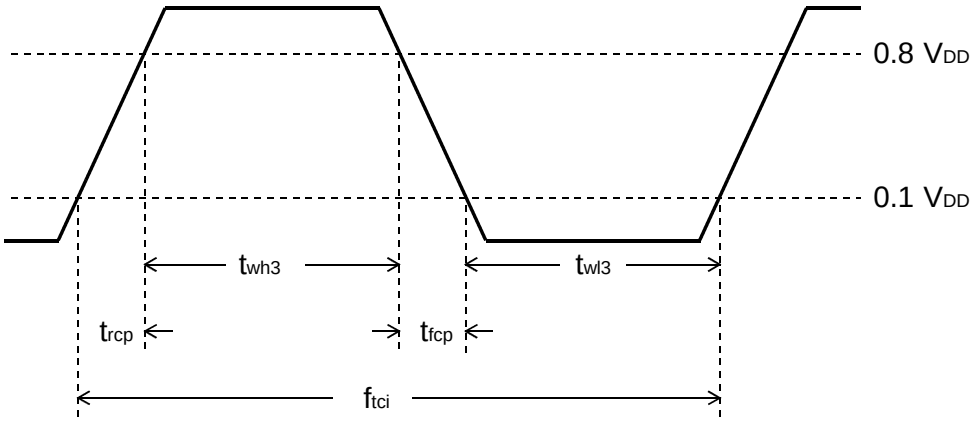


Fig. 4 TCI Timing Chart

C. Electrical Characteristics (DC Characteristics)

Ta= -40 °C to +85 °C, V_{DD}=1.8 V to 5.5 V (V_{RSTL1} or V_{RSTL2} to 5.5 V), V_{SS}=0 V

Parameter		Symbol	Conditions	Limits			Unit
				min	typ	max	
Supply Current							
C1	Operating supply current	I_{DD1}	f_{osc} = 8.0 MHz V_{DD} = 5.0 V		4.0	8.0	mA
		I_{DD2}	f_{osc} = 2.0 MHz V_{DD} = 3.0 V		1.2	2.5	
		I_{DD3}	f_{osc} = 32.768 kHz V_{DD} = 5.0 V		30.0	60.0	µA
C2	Supply current in HALT mode	I_{DD4}	f_{osc} = 32.768 kHz V_{DD} = 5.0 V		15.0	30.0	
C3	Supply current in STOP mode	I_{DD5}	V_{DD} = 5.0 V		0.5	5.0	
C4	Auto reset current consumption	I_{DD6}	V_{DD} = 5.0 V		30.0	80.0	

* Make measurement at Ta = 25 °C while under no-load condition.
* To measure the operating supply current, I_{DD1}, fix the I/O pins to V_{DD} level in the RESET mode, input an 8-MHz square wave, which swings between V_{DD} and V_{SS} voltage levels, into the OSC1 pin.
* To measure the operating supply current, I_{DD2}, fix the I/O pins to V_{DD} level in the RESET mode, input a 2-MHz square wave, which swings between V_{DD} and V_{SS} voltage levels, into the OSC1 pin.
* To measure the operating supply current, I_{DD3}, clear the reset mode and fix the I/O pins to V_{DD} level during execution of NOP instruction, input a 32.768-kHz square wave, which swings between V_{DD} and V_{SS} voltage levels, into the OSC1 pin.
* To measure the supply current in HALT mode, I_{DD4}, clear the RESET mode and set to the HALT mode, and, after fixing the I/O pins to V_{DD} level, input a 32.768-kHz square wave, which swings between V_{DD} and V_{SS} voltage levels, into the OSC1 pin.
* To measure the supply current in STOP mode, I_{DD5}, clear the RESET mode and set to the STOP mode. Then fix the I/O pins to V_{DD} level and open OSC1 pin.
* Auto reset current consumption,I_{DD6}, refers to the constant current consumption of the auto reset circuit with the auto reset function ON selected as a mask option. Therefore, the value of current consumption is added to each supply current rating if the auto reset circuit is enabled.

Ta= -40 °C to +85 °C, V_{DD}=1.8 V to 5.5 V (V_{RSTL1} or V_{RSTL2} to 5.5 V), V_{SS}=0 V

	Parameter	Symbol	Conditions	Limits			Unit
				min	typ	max	
	High-Current I/O Pins P00 to P03 (N-ch open-drain)						
C5	Input voltage high level	V_{IH1}		0.7V_{DD}		V_{DD}	V
C6	Input voltage low level	V_{IL1}		V_{SS}		0.3V_{DD}	
C7	Output leakage current	O_{LK1}	Output: Hi-Z V_{IN} =0 V to 6 V			±10	µA
C8	Output voltage low level	V_{OL1}	I_{OL} =20.0 mA V_{DD} =5.0 V	V_{SS}		2.0	V
	I/O Pins P10 to P13 P20/AD0 to P23/AD3 (When the pins are used as P20 to P23 pins) P30/SYNC/TCI, P31/IRQ/ACZ, P32/TCO/BZ (When the pins are used as P30/SYNC, P31, P32/TCO/BZ pins)						
C9	Input voltage high level	V_{IH2}		0.7V_{DD}		V_{DD}	V
C10	Input voltage low level	V_{IL2}		V_{SS}		0.3V_{DD}	
C11	Input current	I_{I2}	With pull-up resistor V_{IN} = 1.5 V V_{DD} = 5.0 V	-50	-120	-300	µA
C12	Input leakage current	I_{LK2}	Without pull-up resistor V_{IN} = 0 V to V_{DD}			±1	
C13	Output voltage high level	V_{OH2}	I_{OH} = -500 µA V_{DD} = 5.0 V	4.5		V_{DD}	V
C14	Output voltage low level	V_{OL2}	I_{OL} = 3.5 mA V_{DD} = 5.0 V	V_{SS}		0.5	

Note) Use the P30/$\overline{\text{SYNC}}$/TCI pin under the following condition:
The load must be set so that the output voltage high level will be more than 0.8 V_{DD} while the SYNC timing signal is output. That is, at the time the LSI is reset or within two machine cycles after the reset status of the LSI is cleared.

Ta= -40 °C to +85 °C, V_{DD}=1.8 V to 5.5 V (V_{RSTL1} or V_{RSTL2} to 5.5 V), V_{SS}=0 V

Parameter		Symbol	Conditions	Limits			Unit
				min	typ	max	

Input Pins P20/AD0 to P23/AD3 (When the pins are used as A/D input pins)

C15	Converted voltage range	V_{AD}		V_{SS}		V_{DD}	V
C16	Resolution					10	bit
C17	Relative precision		V_{DD} = 5.0 V V_{SS} = 0.0 V			±3	LSB
C18	Zero transition voltage	V_{0T}			10	30	mV
C19	Full-scale transition voltage	V_{FST}			V_{DD} -10	V_{DD} -30	
C20	A/D conversion time		f_{osc} = 8 MHz V_{DD} = 5.0 V V_{SS} = 0.0 V		15.00	27.00 See Note.	µs
C21	Sampling time		f_{osc} = 8 MHz V_{DD} = 5.0 V V_{SS} = 0.0 V		5.00	17.00 See Note.	µs
C22	Analog input voltage	V_{ADIN}		V_{SS}		V_{DD}	V
C23	Analog input leakage current		V_{ADIN}= 0 V to V_{DD} (V_{ADIN} when channel is off.)		±.001	±1	µA
C24	Ladder resistance	R_{ladd}		10	50	100	kΩ

Note) The value is applied when bp3 (ADTC) of the A/D control register ADCL is set to zero.

Relative precision:
The deviation of the converted straight line from the ideal straight line that results after both the zero transition voltage and full-scale transition voltage are adjusted to zero.

Zero transition voltage:
Indicates the difference between the analog input voltage and the nominal value when the digital output code changes from 0 (000h) to 1 (001h).

Full-scale transition voltage:
Indicates the difference between the analog input voltage and the nominal value when the digital output code (3FEh) reaches the full-scale value (3FFh).

Ta= -40 °C to +85 °C, V_{DD}=1.8 V to 5.5 V (V_{RSTL1} or V_{RSTL2} to 5.5 V), V_{SS}=0 V

Parameter	Symbol	Conditions	Limits			Unit
			min	typ	max	

Input Pin P31/$\overline{IRQ}$/ACZ (When this pin is used as ACZ pin)

C25	ACZ input (high-level output)	V_{SH}	Fig. 5	1.5		V_{DD} -1.5	V
C26	ACZ input (low-level output)	V_{SL}	V_{DD}=4.5 V to 5.5 V	V_{SS}		0.5	
				V_{DD} -0.5		V_{DD}	
C27	Input leakage current	I_{LK3}	Without pull-up resistor V_{IN} = 0 V to V_{DD}			±1	µA
C28	Input clamp current	I_{C3}	V_{IN} > V_{DD} V_{IN} > V_{SS} V_{DD} = 5.0 V			±400	

I/O Pin P31/$\overline{IRQ}$/ACZ (Schmitt input when this pin is used as $\overline{IRQ}$ pin)

C29	Input voltage high level	V_{IH4}		0.8V_{DD}		V_{DD}	V
C30	Input voltage low level	V_{IL4}		V_{SS}		0.1V_{DD}	
C31	Input current	I_{I4}	With pull-up resistor V_{IN} = 1.5 V V_{DD} = 5.0 V	-50	-120	-300	µA
C32	Input leakage current	I_{LK4}	Without pull-up resistor V_{IN} = 0 V to V_{DD}			±1	

I/O Pin P30/$\overline{SYNC}$/TCI (Schmitt input when this pin is used as TCI pin)

C33	Input voltage high level	V_{IH5}		0.8V_{DD}		V_{DD}	V
C34	Input voltage low level	V_{IL5}		V_{SS}		0.1V_{DD}	
C35	Input current	I_{I5}	With pull-up resistor V_{IN} = 1.5 V V_{DD} = 5.0 V	-50	-120	-300	µA
C36	Input leakage current	I_{LK5}	Without pull-up resistor V_{IN} = 0 V to V_{DD}			±1	

Ta= -40 °C to +85 °C, V_{DD}=1.8 V to 5.5 V (V_{RSTL1} or V_{RSTL2} to 5.5 V), V_{SS}=0 V

	Parameter	Symbol	Conditions	Limits			Unit
				min	typ	max	
I/O Pin $\overline{RST}$ (Schmitt input)							
C38	Input voltage high level	V_{IH6}		0.8V_{DD}		V_{DD}	V
C39	Input voltage low level	V_{IL6}		V_{SS}		0.1V_{DD}	
C40	Input current	I_{I6}	With pull-up resistor V_{IN} = 1.5 V V_{DD} = 5.0 V	-50	-120	-300	µA
C41	Input leakage current	I_{LK6}	Without pull-up resistor V_{IN} = 0 V to V_{DD}			±1	
C42	Output voltage low level	V_{OL6}	V_{DD} = 2 V, I_{OL} = 0.3 mA	V_{SS}		0.4	V

D. Electrical Characteristics (AC Characteristics)

Ta= -40 °C to +85 °C, V_{DD}=1.8 V to 5.5 V (V_{RSTL1} or V_{RSTL2} to 5.5 V), V_{SS}=0 V

Parameter		Symbol	Conditions	Limits			Unit
				min	typ	max	
$\overline{RST}$ Pin							
D1	Effective pulse width	t_{wRST}	Fig. 5	1			mc

* The above pin may not be reset if the pulse width is shorter than the effective pulse width.

(mc: Machine cycle)

P31/$\overline{IRQ}$/ACZ (When this pin is used as ACZ pin)

D2	Rise time	t_{rs}	Fig. 6	30			µs
D3	Fall time	t_{fs}		30			

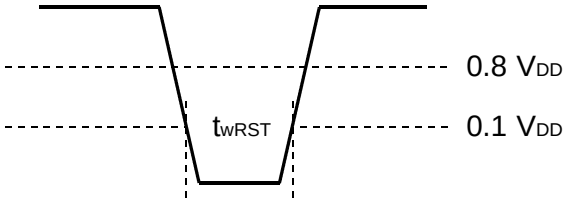


Fig. 5 RST Input Pulse Width

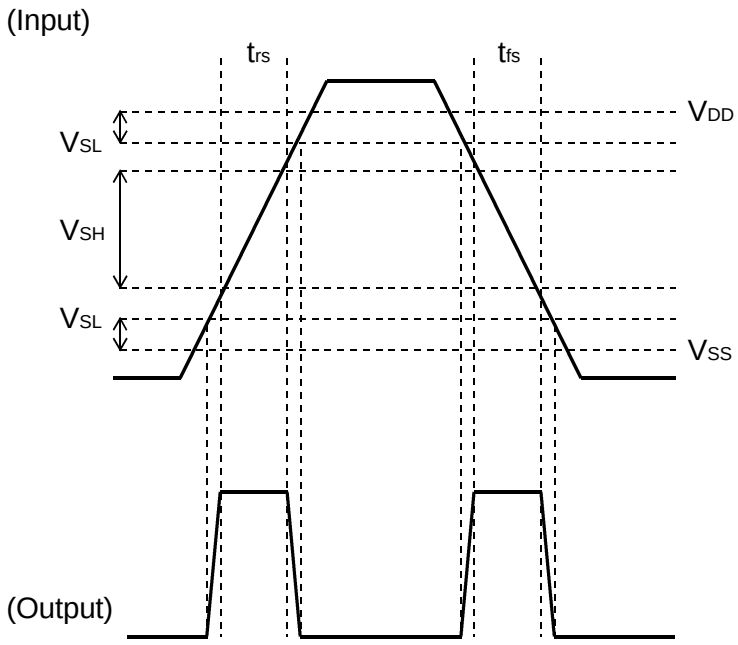
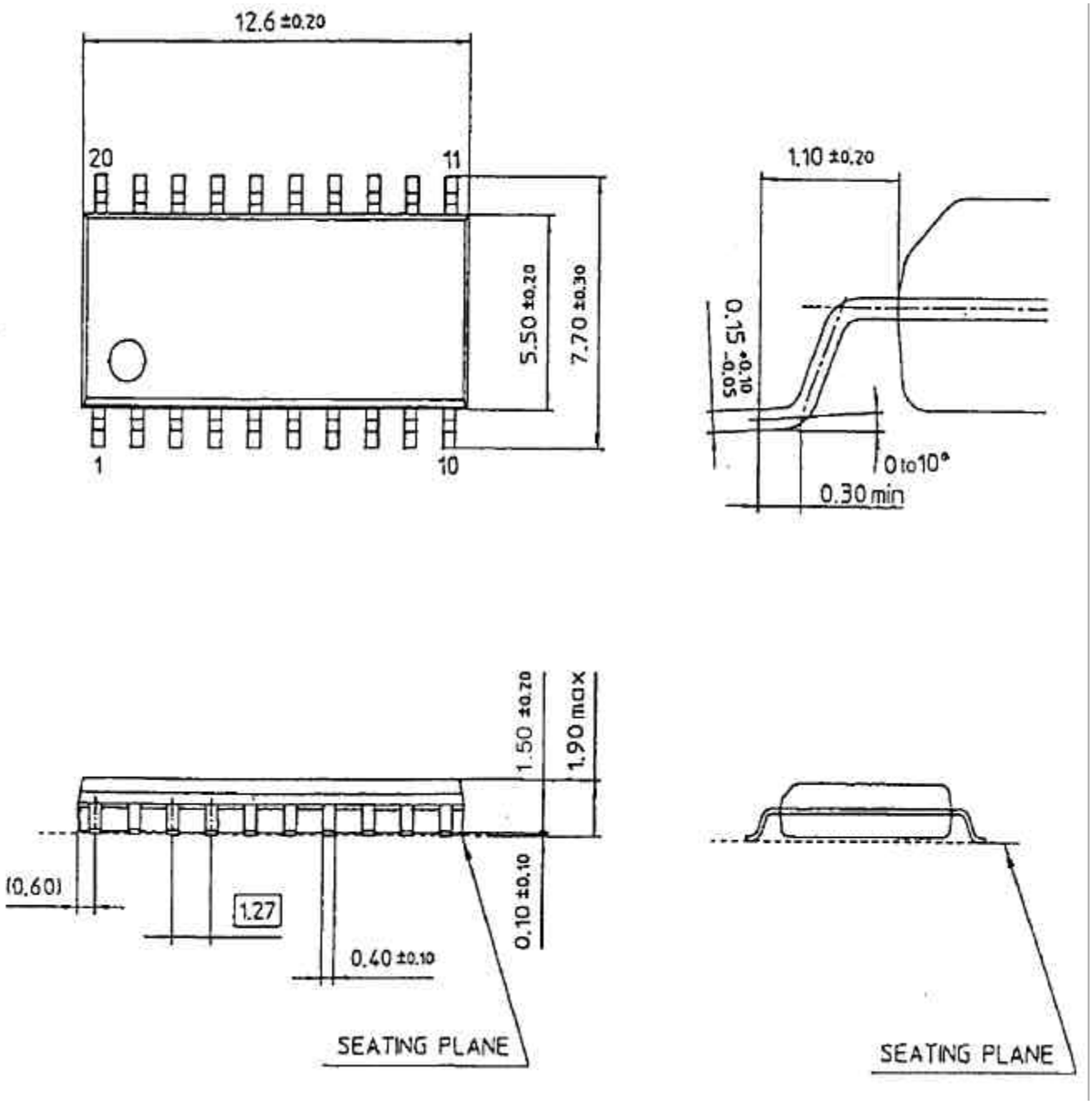


Fig. 6 AC Zero Voltage Detection Circuit Operating Diagram

1.8 Package

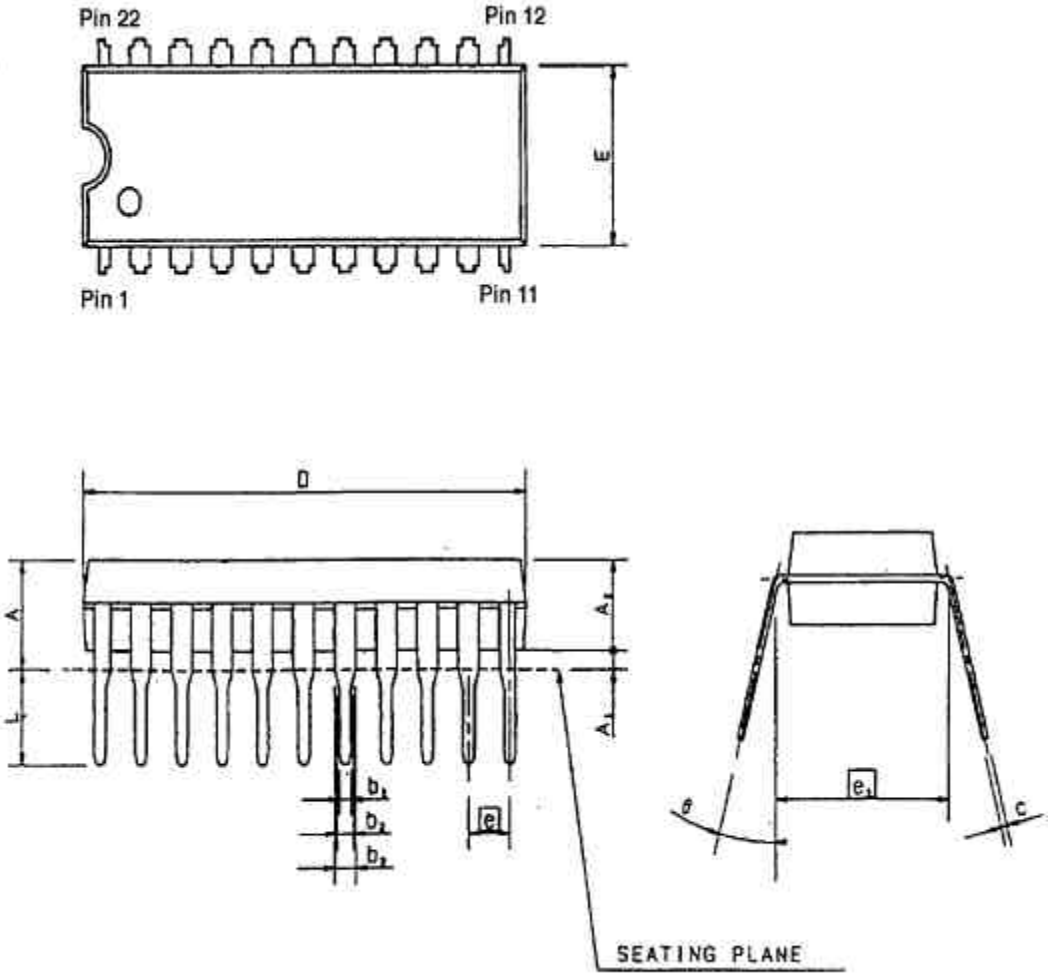
Package 1

PACKAGE CODE: SOP020-P-0300



Package 2

PACKAGE CODE: SDIP022-P-0300



Symbol	Dimension in Millimeters		
	min	typ	max
A	——	——	4.8
A_1	0.7	——	——
A_2	3.1	3.3	3.5
b_1	0.4	0.5	0.6
b_2	0.6	0.7	0.8
b_3	0.8	0.9	1.0
c	0.2	0.25	0.45
D	18.8	19.2	19.6
E	6.2	6.4	6.6
e	——	(1.778)	——
e_1	7.42	7.62	7.82
L	3.15	3.45	3.75
θ	0	——	15(0.262rd)

Mask Option Check List

Part No.	MN150222

1. Operating supply voltage range

	Operating voltage range	Usage	
		Used	Unused
Operating mode	V to V	----	----
HALT mode	V to V		
STOP mode	V to V		

2. Clock

Oscillation mode	Xtal	
Oscillator frequency	32 kHz to 125 kHz in low-speed oscillation mode	0.5 MHz to 8 MHz in high-speed oscillation mode
Remarks		

3. Auto reset function

* Use the LSI in auto reset function ON mode with one machine cycle set to 4.0 ms or more when V_{RSTL1} reset voltage is selected and 8.0 ms or more when V_{RSTL2} reset voltage is selected.

Auto reset function	
ON	OFF

Mark "✓" on the corresponding item if ON is selected.

Reset voltage	
V_{RSTL1}	V_{RSTL2}
2.0 V to 4.0 V (Use the LSI at normal 5-V supply voltage.)	1.2 V to 2.6 V (Use the LSI at normal 3-V supply voltage.)

4. Pull-up resistor at reset pin

ON	OFF

5. Watchdog timer function

ON	OFF

6. A/D conversion function

ON	OFF

7. AC zero voltage detection function

ON	OFF

8.1 Pin Structure

Pin name			Function				
P10			Output type selection		N-ch open-drain		Push-pull
			Pull-up resistor		ON		OFF
P11			Output type selection		N-ch open-drain		Push-pull
			Pull-up resistor		ON		OFF
P12			Output type selection		N-ch open-drain		Push-pull
			Pull-up resistor		ON		OFF
P13			Output type selection		N-ch open-drain		Push-pull
			Pull-up resistor		ON		OFF
P20/AD0 Note 1)		P20	Output type selection		N-ch open-drain		Push-pull
			Pull-up resistor		ON		OFF
		AD0	Output type selection		N-ch open-drain		Push-pull
			Pull-up resistor	X	ON	✓	OFF
P21/AD1 Note 1)		P21	Output type selection		N-ch open-drain		Push-pull
			Pull-up resistor		ON		OFF
		AD1	Output type selection		N-ch open-drain		Push-pull
			Pull-up resistor	X	ON	✓	OFF
P22/AD2		P22	Output type selection		N-chopen-drain		Push-pull
			Pull-up resistor		ON		OFF
		AD2	Output type selection		N-ch open-drain		Push-pull
			Pull-up resistor	X	ON	✓	OFF
P23/AD3 Note 1)		P23	Output type selection		N-ch open-drain		Push-pull
			Pull-up resistor		ON		OFF
		AD3	Output type selection		N-ch open-drain		Push-pull
			Pull-up resistor	X	ON	✓	OFF

Note 1) A pull-up resistor cannot be connected to the pin when AD pin is selected on PTAD2-0 of ADCH X 'A' , A/D Control Register.

8.2 Pin Structure

Pin name	Function				
P30/$\overline{\text{SYNC}}$/TCI	Output type selection		N-ch open-drain		Push-pull
	Pull-up resistor		ON		OFF
P31/$\overline{\text{IRQ}}$/ACZ Note 2)	Output type selection		N-ch open-drain		Push-pull
	Pull-up resistor		ON		OFF
P32/TCO/BZ	Output type selection		N-ch open-drain		Push-pull
	Pull-up resistor		ON		OFF

Note 2) A pull-up resistor cannot be connected when the AC zero voltage detection function is used.

CHAPTER 2 CPU CORE FUNCTIONS

2.1 Clock Generator and CPU Basic Timing

This LSI incorporates the system clock oscillation circuits (OSC1 and OSC2). The circuit has an oscillation element and capacitors connected externally. A Xtal oscillator or a ceramic oscillator is utilized as the oscillation element.
When mounting the LSI on PCB, design a pattern so that the oscillation elements and capacitors will be arranged as physically close to the LSI as possible.
Also provide a thick ground line that can be connected to V_{SS} with the LSI at the shortest distance possible. Note that long wiring pattern is susceptible to noise interference and results in unstable oscillation. Fig. 2.1.1 shows a connection diagram. Optimum values for the capacitors differ depending on the oscillator used. Use the values specified by each oscillator maker.

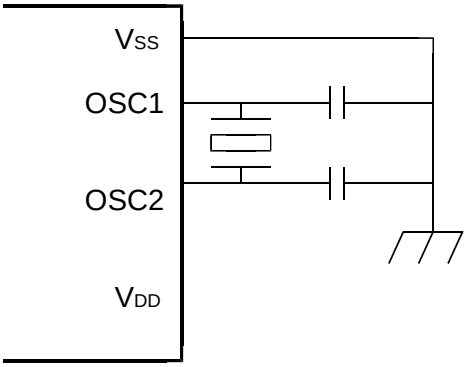


Fig. 2.1.1 Oscillation Circuit Connection Diagram

This LSI constitutes a machine cycle (state) with 4-phase clocks, S0, S1, S2 and S3, generated from the oscillation source (OSC1 and OSC2).
One machine cycle is 1.0 μs when oscillation source, f_{osc}, is 8.0 MHz.

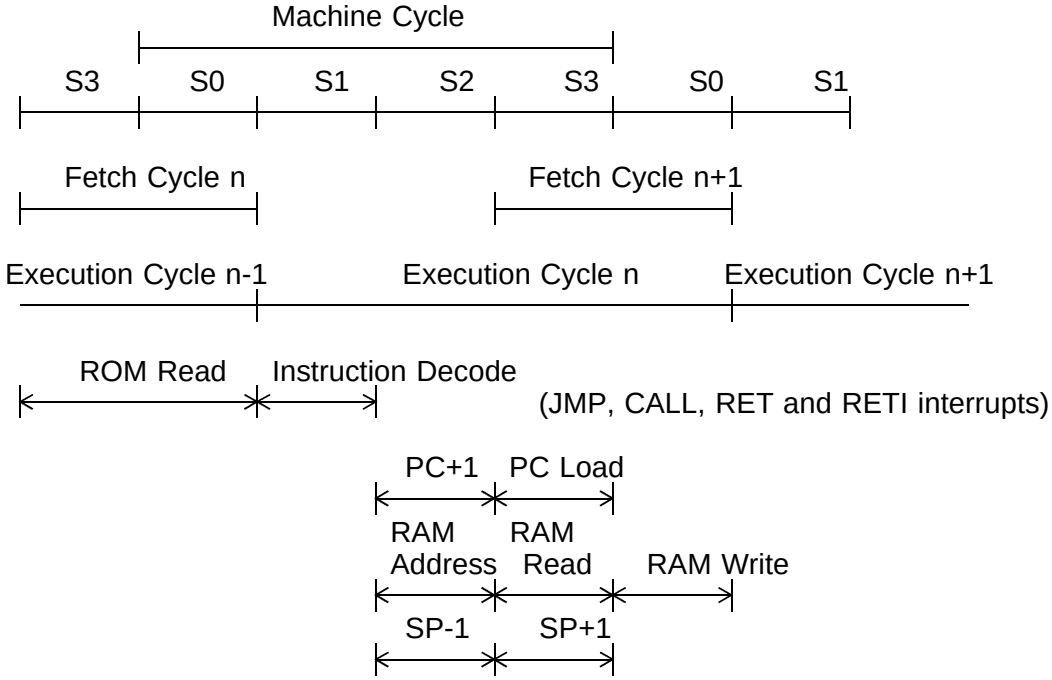


Fig. 2.1.2 Machine Cycle and CPU Basic Timing

2.2 ROM and RAM

This LSI has a 2-Kbyte instruction memory space (ROM) to store instructions, and a 96-nibble (including a 32-nibble stack area) data memory space (RAM) to store data separately from each other.
Fig. 2.2.1 shows the ROM address space and Fig. 2.2.2 shows the RAM address space.

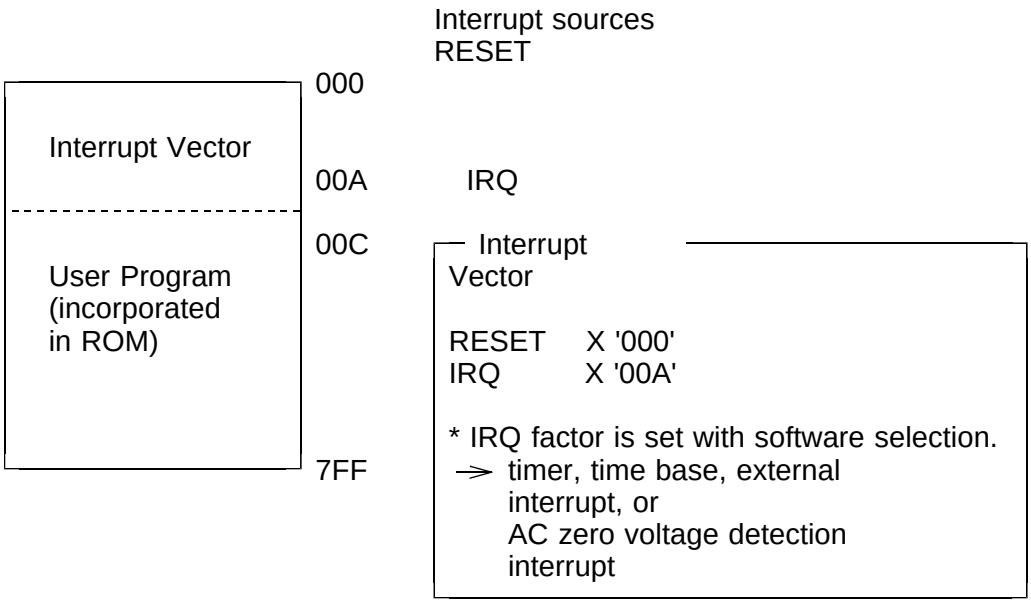


Fig. 2.2.1 ROM Address Space

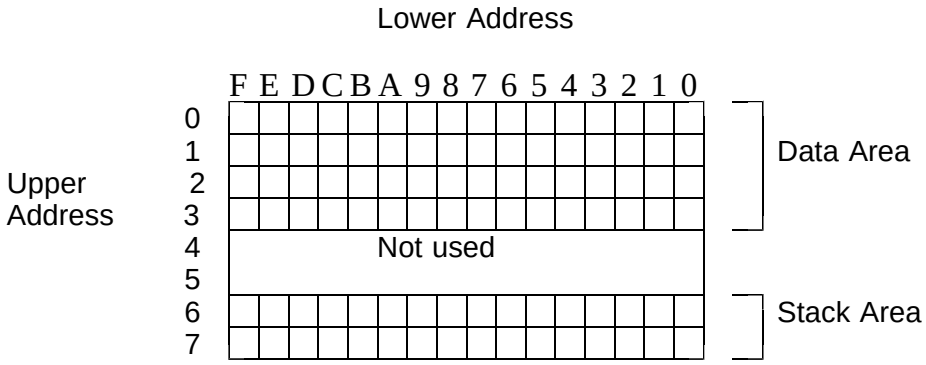


Fig. 2.2.2 RAM Address Space

2.3 Stack Area

This LSI has assigned as a stack area the addresses (6, 0) to (7, F) in the RAM area. The stack area is used to save the PC (Program Counter), flag statuses (ZF and CF) and A, X and Y registers at the time of the CALL instruction, PSH instruction or an interrupt.
When the entire stack area is not used, it is also available as regular RAM. When only the CALL instruction is executed, up to 8 levels can be used.
Fig. 2.3.1 shows the stack condition when the CALL instruction, PSH instruction or an interrupt sequence is executed.

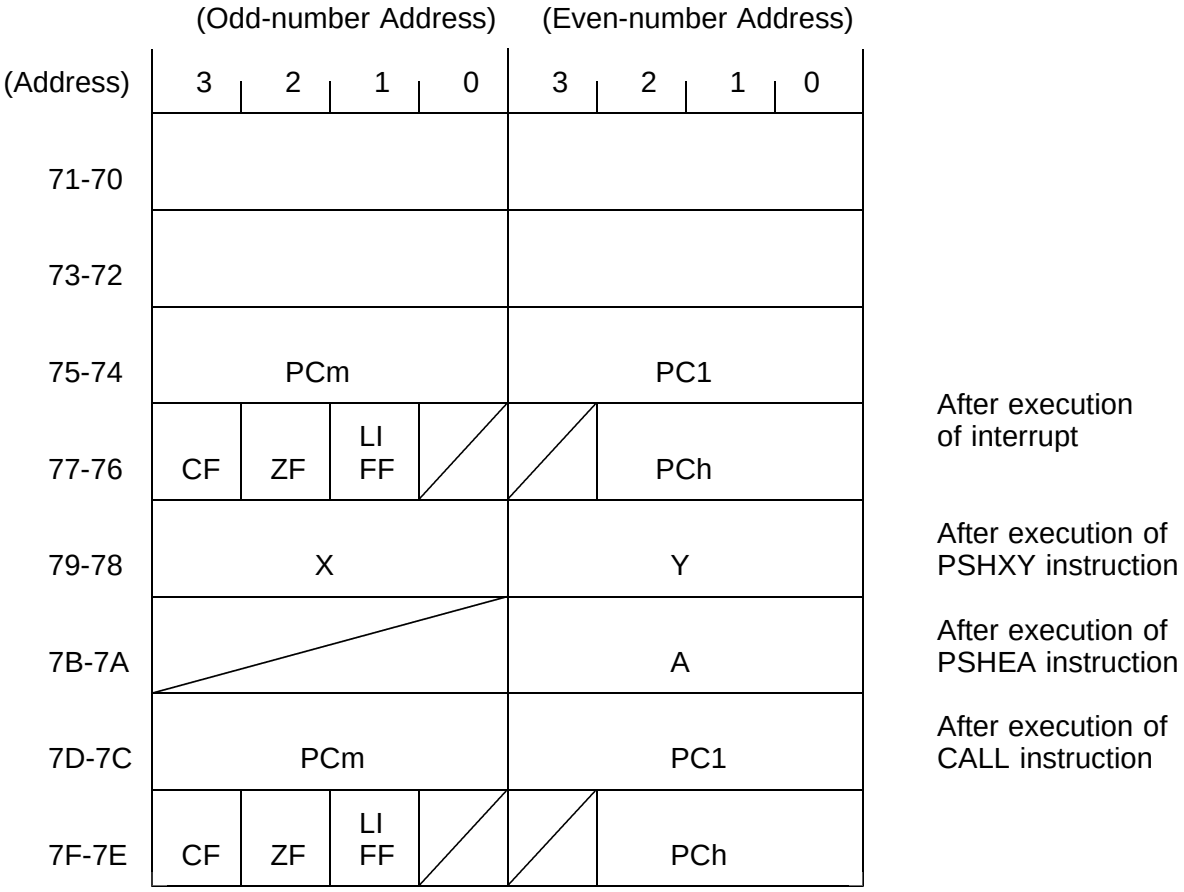


Fig. 2.3.1 Stack Area Condition

Note 1) At reset time, the SP (Stack Pointer) points to 60. The stack data are used sequentially, starting at address 7F to 60.
Note 2) The RET instruction does not return the flags (CF, ZF and LIFF). Only the RETI instruction is returned.
Note 3) LIFF: This is FF to memorize that the instruction just before was LI. It is used for an LI instruction stacking function.
Note 4) The values in the oblique-lined cells in Fig. 2.3.1 are indefinite.

2.4 Flag Status

The flag status is composed of a 2-bit register consisting of the arithmetic flags, that is, carry flag (CF) and zero flag (ZF). CF is set when an arithmetic result of the ALU overflows or underflows, or is otherwise reset. ZF is set when the arithmetic result of the ALU is zero, or is otherwise reset.

2.5 Backup Mode

In order to reduce power consumption, there are two kinds of backup modes provided, which can be controlled by the program.

- HALT mode: The system clock frequency divider is operating. However, system clock is not supplied. It is returned by a reset operation or an interrupt.
- STOP mode: The power consumption can be reduced further because the system clock frequency divider is also stopped. As with the HALT mode, it is returned by a reset operation or an interrupt. (Software option)

Table 2.5.1 shows the STOP and HALT functions.

Table 2.5.1 STOP and HALT Functions

Mode / Operation	STOP	HALT
Operating condition	1) The system clock oscillation circuit stops. 2) Timer/Counter - It is operating in event count mode. - It is stopped in timer mode. 3) Time base is stopped.	1) The system clock oscillation circuit is operating. (System clock frequency divider is operating. However, system clock is not supplied.) 2) Timer/Counter - It is operating in event count mode. - It is operating when the clock is $f_{osc}/2^{14}$ in timer mode. - It is operating when the clock is $f_{sys}/2$ in timer mode. 3) Time base is operating.
Register/RAM condition	Holds the contents of the RAM and all registers.	
Mode setting method	Executes a WI instruction just after an EDI instruction. (Refer to Example: 2.5.1.)	Executes the WI instruction after an instruction other than an EDI instruction. (Refer to Example: 2.5.2.)
Return	- Interrupt: Identical operation with a normal interrupt - Reset : Identical operation with a normal reset	

Example: 2.5.1 Using the STOP Mode

```
        ⋮
ED  0.4     Exits from the STOP mode when an IRQ (external interrupt) occurs.
WI
NOP         Be sure to insert one or more NOPs next to the EDI and WI instructions
            in order to stabilize operation.
        ⋮
```

Note) Following is an interrupt which enables return from the STOP mode.
IRQ (External interrupt, ACZ interrupt or timer in the event count mode.)

Example: 2.5.2 Using the HALT Mode

```
        ⋮
    EDI   0.4        Returns from the HALT mode when an interrupt occurs.
  (Instruction other than
  EDI instruction)
        ⋮
    WI
    NOP
        ⋮
```

Note) Be sure to insert one or more NOPs next to the WI instruction. The currently provided cross assembler inserts an NOP automatically.

Table 2.5.2 shows the comparison of STOP and HALT modes.

Table 2.5.2 STOP and HALT Modes Comparison Table

	OSC	IRQ	CPU	RESET
STOP mode	-	✓ (Note 1)	-	✓
HALT mode	✓	✓ (Note 2)	-	✓

✓ : Operates - : Stops

Unless the MASKIR bit is set to zero, IRQ does not operate.

Note 1) The timer interrupt function operates in event count mode and does not operate in timer mode. The time base interrupt function does not operate in STOP mode.
Note 2) The timer interrupt function operates in event count mode or timer mode with the clock source of $f_{osc}/2^{14}$ selected but does not operate in timer mode with the clock source of $f_{sys}/2$ selected. The time base interrupt function, however, operates.

Precautions for using the Backup Mode

1. Handling of the output ports
   In the backup mode, the port level can be made floating in order to reduce power consumption at the output ports. The port status can be set by controlling the corresponding bit of the control register. (Refer to Table 2.5.3.)

Table 2.5.3 Interrupt Mode Register (CPUM: X'4' R/W) versus Output Ports

HIZC	Port Status
1	All output pins are floating (Hi-Z) Note) The voltage level is set to "H" if a pull-up resistor is selected as a mask option.
0	Normal output

(Set to "1" in RESET mode)

2. Handling of the input ports
   A pull-up resistor for the input port should be specified according to the external circuit voltage level in the backup operation, in order to reduce power consumption at the port. Set the input port voltage level externally so that it will be turned to either "L" or "H" level in the backup operation. When the port is at the middle level, a current flows internally and the microcomputer consumes more power.

3. Return from the STOP mode
   When the supply voltage is less than 1.8 V at the time of return, the RAM data cannot be guaranteed after return. If this is the case, reset by means of an external circuit or use the auto reset function.

4. Handling of the I/O ports
   After first setting to the Hi-Z state, set the I/O ports externally so that the pin levels will be turned to "L" or "H" level. When they are at the middle level, the microcomputer consumes more power.

5. Handling of the A/D Control Registor
   Setting from outside is not needed when A/D input is unused on AD, because P2 input gate is fixed to stop feedthrough current. The pin which selects AD cannot be connected to a pull-up resistor as a mask option.

2.6 Reset

The LSI is reset with the $\overline{RST}$ pin set to "L" level. When the LSI is reset, the register and output port latch are initialized as shown in table 2.6.1.
The $\overline{RST}$ pin should be set to "L" level for a machine cycle or more for stabilized reset operation, otherwise the LSI may not be reset.

Table 2.6.1 Initial Values of Registers and Data Memories

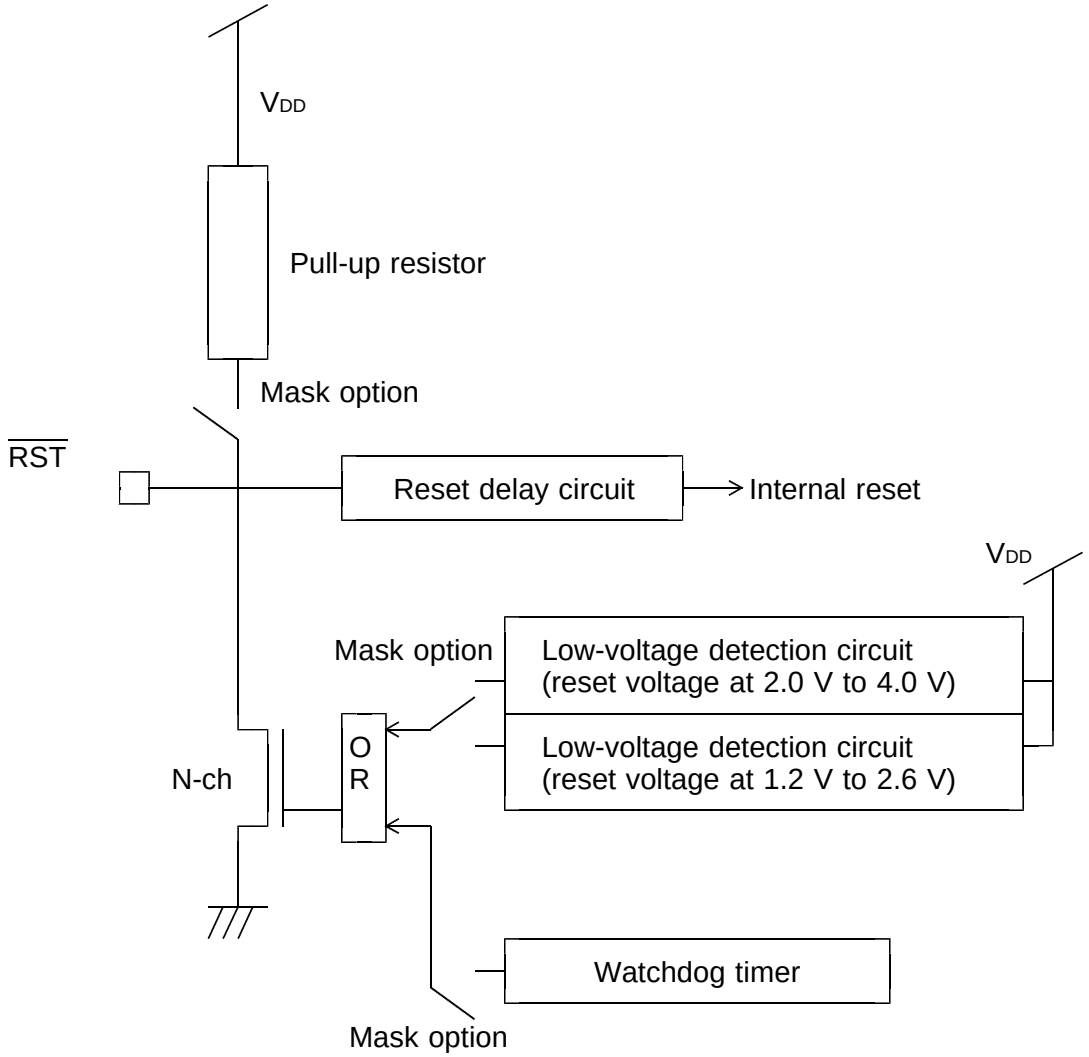
Register/Memory	Symbol	Initial Value	Register/Memory	Symbol	Initial Value
Program counter	PC	✓	Interrupt accept flag	IF	✓
Accumulator	A	✓	Interrupt enable/disable flag	IE	Disabled
Register X	X	✓	Output port latch		1
Register Y	Y	✓	I/O register	IR	1
Carry flag	CF	✓			
Zero flag	ZF	✓			
RAM		Indefinite			
Stack pointer	SP	60			

[Reset Clearing Timing]

This LSI clears an internal reset by counting 2^{14} pulses (2^7 pulses in low-speed mode) worth of OSC input clock after the $\overline{RST}$ pin is turned to "H". This is because the microcomputer may malfunction if a reset is cleared when the oscillation source of system clock is unstable.
When designing a system, design the reset timing taking the above point into account. Refer to Fig. 2.7.2.

2.6.1 Auto Reset Function (Mask Option)

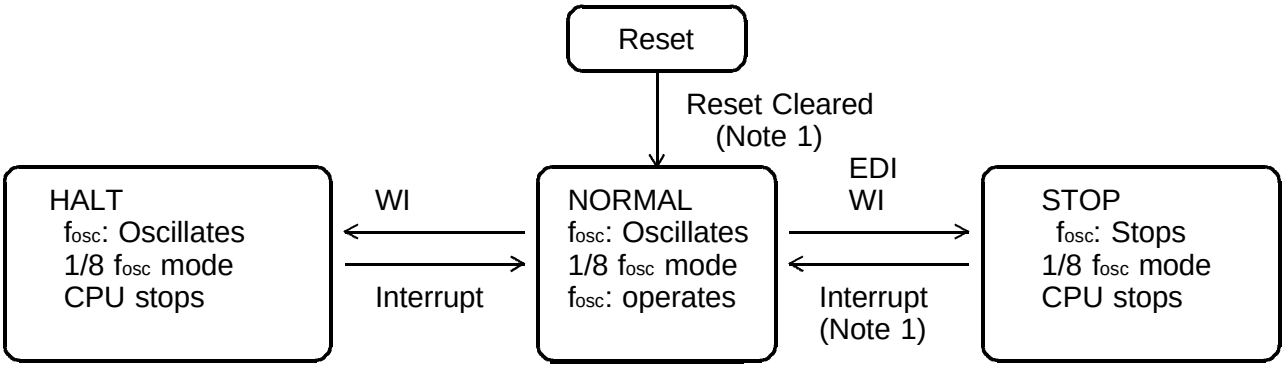
The auto reset circuit is enabled or disabled according to the mask option.
The auto reset function enables the low-voltage detection circuit to operate and sets the $\overline{RST}$ pin to "L" level when the V_{DD} drops to or below V_{RSTL} level. The following diagram shows the auto reset block.



2.7 Clock Switching Function

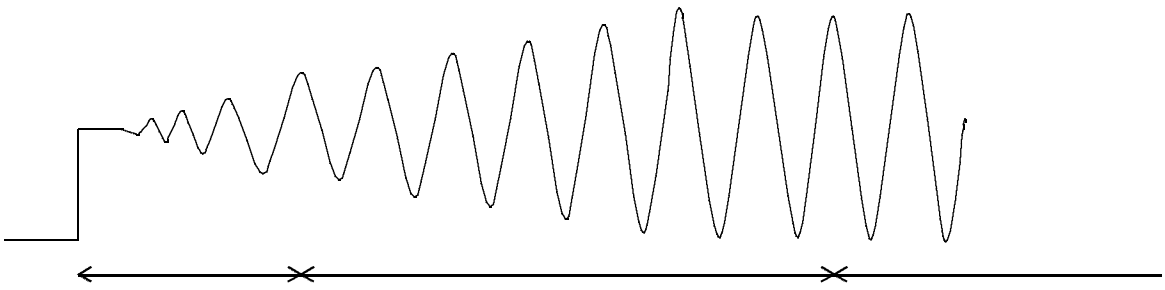
The LSI operates in high- or low-speed Xtal oscillation mode according to the mask option. As shown in Fig. 2.7.1, the oscillation starts from the reset cycle when the LSI is reset. At CPU reset time, a hardware-wise waiting time, $t_{wait\ (osc)}$, takes place in the return from STOP mode automatically until the clock oscillation is stabilized.
The waiting time, $t_{wait\ (osc)}$, on the oscillator side is a period in which 2^{14} pulses are counted in high-speed Xtal oscillation mode and 2^7 pulses are counted in low-speed Xtal oscillation mode after the oscillation starts.
The clock oscillation starting time of the LSI varies with the type of crystal and the value of the oscillation circuit capacitor. Generally, the lower the oscillator frequency is, the slower the starting time is. For example, it requires a few hundreds of milliseconds at 32 kHz, which should be taken into consideration to design the system. Refer to Fig. 2.7.1.

Fig. 2.7.1 CPU Operation Modes and Settings



Note 1) The hardware awaits the stabilization of OSC oscillation.

Fig. 2.7.2 Wait at Oscillation Start



$$t_{wait}=2^{14}\times\frac{1}{f_{osc}}$$ (High-speed Xtal oscillation mode)

$$t_{wait}=2^{7}\times\frac{1}{f_{osc}}$$ (Low-speed Xtal oscillation mode)

CHAPTER 3 I/O REGISTER FUNCTIONS

3.1 I/O Registers List

Address	Name	Function
X'0'	PORT0	P0 port register
X'1'	PORT1	P1 port register
X'2'	PORT2	P2 port register
X'3'	PORT3	P3 port register
X'4'	CPUM	CPU control
X'5'	TBL	Timer control (Timer buffer lower 4 bits)
X'6'	TBH	Timer control (Timer buffer upper 4 bits)
X'7'	TM	Timer control (Timer mode)
X'8'	TMBC	Time base control
X'9'	ADCL	A/D control
X'A'	ADCH	A/D control
X'B'	ADDL	A/D control (A/D buffer lower 2 bits)
X'C'	ADDM	A/D control (A/D buffer middle 4 bits)
X'D'	ADDH	A/D control (A/D buffer upper 4 bits)
X'E'	Not used	———
X'F'	IRQC	Interrupt selection

3.2 Allocation and Description of Registers

3.2.1 I/O Port Registers

Data output to the pin is done by writing the output data into the port register, and data input from the pin is done by reading the data from the port register. Each register consists of 4 bits (one port worth).

Address	Name	Port	I/O	Description
X'0'	PORT0	P0	I/O	4-bit parallel data I/O port. The output is N-ch open-drain type. Capable of directly driving the LED.
X'1'	PORT1	P1	I/O	4-bit parallel data I/O port. The output type and a pull-up resistor connection can be specified by a mask option.
X'2'	PORT2	P2	I(P20) I/O	4-bit parallel data I/O port. The P20 to P23 are used in common with AD0 to AD3 respectively. The output type and a pull-up resistor connection can be specified by a mask option.
X'3'	PORT3	P3	I/O	4-bit parallel data I/O port. The P30 is shared with the $\overline{\text{SYNC}}$ and TCI (timer input). The P31 is shared with the $\overline{\text{IRQ}}$ and ACZ. The P32 is shared with the TCO (timer output) and BZ (buzzer) output.

3.2.2 CPU Control Register

The Hi-Z control of all I/O pins is specified through the CPU control register. So are the control of the watchdog timer operation and the system clock frequency dividing ratio.

CPUM X '4' R/W (bit 1 is write-only.)

bit	Name	Description	Initial Value
0	HIZC	Specifies Hi-Z for all output pins. See Note 1. 1: Sets all the pins to Hi-Z. 0: Clears Hi-Z control for all the pins.	1
1	WDEN	Specifies the operation of the watchdog timer. See Note 2. 1: Clear 0: Enabled	0
2	—	Always set to 1.	1
3	—	Unused	—

Note 1) Hi-Z control does not apply to the $\overline{\text{SYNC}}$ pin and pull-up selection pin.
Note 2) If WDEN is set to 1, the counter clear signal is output for one machine cycle. Then WDEN is set to 0 and the watchdog timer restarts, provided that the watchdog timer is selected as a mask option.

3.2.3 Timer Control Registers

This LSI incorporates an 8-bit timer.

Address	Name	Configuration	Function	Initial Value
X '5'	TBL	R/W Note)	Timer buffer lower 4 bits	F
X '6'	TBH	R/W Note)	Timer buffer upper 4 bits	F
X '7'	TM	R/W	Timer mode register	F
X '8'	TMBC	R/W	Time base mode register	Indefinite

Note) The value of the binary counter is read out at register read time.

(1) Timer buffer

This is a register to set the data to the timer binary counter. Since the value of the binary counter is read out at register read time, a value different from the written one may be read out while the timer is operating.

TBL X '5' R/W

bit	Description	Initial Value
0 to 3	Timer buffer lower 4 bits	F

TBH X '6' R/W

bit	Description	Initial Value
0 to 3	Timer buffer upper 4 bits	F

(2) Timer Mode Registers

The timer mode register is used to set the clock source and operation mode of timer.

TM X '7' R/W

<table>
<tr><th>bit</th><th>Name</th><th>Description</th><th>Initial Value</th></tr>
<tr><td>0</td><td>TMEN</td><td>Specifies timer operation.
1: The timer stops.
0: The timer operates.</td><td>1</td></tr>
<tr><td>1</td><td>TCOE</td><td>Selects P32, TCO or BZ.
(Selects port I/O, timer output or buzzer output.)
1: Selects P32/BZ (port I/O or buzzer output).
0: Selects TCO (timer output).
Note) Selects P32 or BZ with bit 1 (BZOE) of the X'8' port register.</td><td>1</td></tr>
<tr><td>2</td><td>CLK0</td><td rowspan="2">Selects the clock of timer.
<table>
<tr><th>CLK0</th><th>CLK1</th><th>Clock Source</th></tr>
<tr><td>0</td><td>0</td><td>TCI input/2^6
See Note 1.</td></tr>
<tr><td>0</td><td>1</td><td>TCI input
See Note 1.</td></tr>
<tr><td>1</td><td>0</td><td>$f_{osc}/2^{14}$</td></tr>
<tr><td>1</td><td>1</td><td>$f_{sys}/2$
See Notes 2 and 3.</td></tr>
</table></td><td>1</td></tr>
<tr><td>3</td><td>CLK1</td><td>1</td></tr>
</table>

Note 1) The P30/$\overline{\text{SYNC}}$/TCI output is set to Hi-Z.
Note 2) $f_{sys} = 1/8f_{osc}$.
Note 3) If $f_{sys}/2$ is selected, the timer stops when the LSI is in HALT mode.

3.2.4 Time Base Control Register

This LSI incorporates a time base besides an 8-bit timer.

(1) Time Base Mode Register

This register is used for the selection of time base output and clock source setting.

TMBC X '8' R/W (bit 0 is read-only)

<table>
<tr><th>bit</th><th>Name</th><th>Description</th><th>Initial Value</th></tr>
<tr><td>0</td><td>TMB</td><td>When the IN instruction is executed, the clock frequency, which is selected by the BZSEL0 and BZSEL1 bits, is set in bit 0 of the accumulator.</td><td>Indefinite</td></tr>
<tr><td>1</td><td>BZOE</td><td>Selects P32, TCO or BZ.
1: Selects P32.
0: Selects BZ (buzzer output).
Note) The setting in the BZOE bit is disabled if TCO output is selected with the TCOE bit.</td><td>1</td></tr>
<tr><td>2</td><td>BZSEL0</td><td rowspan="2">Selects clock output to be provided to the buzzer and time base.
<table>
<tr><th>BZSEL0</th><th>BZSEL1</th><th>Clock Source</th></tr>
<tr><td>1</td><td>1</td><td>$f_{osc}/2^{12}$</td></tr>
<tr><td>1</td><td>0</td><td>$f_{osc}/2^{11}$</td></tr>
<tr><td>0</td><td>1</td><td>$f_{osc}/2^{10}$</td></tr>
<tr><td>0</td><td>0</td><td>$f_{osc}/2^{9}$</td></tr>
</table></td><td>1</td></tr>
<tr><td>3</td><td>BZSEL1</td><td>1</td></tr>
</table>

3.2.5 A/D Control Register

This LSI incorporates a 4-channel A/D converter.
The LSI uses a total of eight registers for channel selection, starting A/D conversion, or stopping A/D conversion.

ADCL X '9' R/W

<table>
<tr><th>bit</th><th>Name</th><th>Description</th><th>Initial Value</th></tr>
<tr><td>0</td><td>ADCHS0</td><td rowspan="4">Selects the channel for A/D conversion.
<table><tr><th>ADCHS1</th><th>ADCHS0</th><th>Channel</th></tr><tr><td>1</td><td>1</td><td>AD0</td></tr><tr><td>1</td><td>0</td><td>AD1</td></tr><tr><td>0</td><td>1</td><td>AD2</td></tr><tr><td>0</td><td>0</td><td>AD3</td></tr></table></td><td>1</td></tr>
<tr><td>1</td><td>ADCHS1</td><td>1</td></tr>
<tr><td>2</td><td>ADSTAT</td><td>Indicates the operation status of A/D conversion.
1: A/D conversion is completed or is not in process.
0: A/D conversion has started or is in process.</td><td>1</td></tr>
<tr><td>3</td><td>ADTC</td><td>Selects the A/D conversion rate.
1: 15 machine cycles
0: 27 machine cycles</td><td>1</td></tr>
</table>

ADDH X 'A' R/W

<table>
<tr><th>bit</th><th>Name</th><th>Description</th><th>Initial Value</th></tr>
<tr><td>0</td><td>PTAD0</td><td rowspan="3">Selects P20 to P23 or AD0 to AD3 signals.
<table><tr><th>PTAD0</th><th>PTAD1</th><th>PTAD2</th><th>Setting</th></tr><tr><td>0</td><td>0</td><td>0</td><td>Selects AD0 to AD3</td></tr><tr><td>1</td><td>0</td><td>0</td><td>Selects AD0 to AD2 and P23</td></tr><tr><td>0</td><td>1</td><td>0</td><td>Selects AD0, AD1, P22 and P23</td></tr><tr><td>1</td><td>1</td><td>0</td><td>Selects AD0 and P21 to P23</td></tr><tr><td>*</td><td>*</td><td>1</td><td>Selects P20 to P23</td></tr></table>*: Don't care</td><td>1</td></tr>
<tr><td>1</td><td>PTAD1</td><td>1</td></tr>
<tr><td>2</td><td>PTAD2</td><td>1</td></tr>
<tr><td>3</td><td>ADHAL</td><td>Disconnects the reference power supply in order to save the current consumption of the A/D converter.
1: A/D converter not in use.
0: A/D converter in use.</td><td>1</td></tr>
</table>

Note) When the A/D converter is in use, set the analog data input pins to analog data input only mode. On that occasion, the pin which selects AD cannot be connented to a pull-up resister. To set the LSI to low-current consumption mode (i.e., STOP or HALT mode), set the ADHALT bit to 1.

(1) A/D Buffer

The following A/D buffers are used for storing the results of A/D conversion.

ADDL X 'B' R

bit	Name	Description	Initial Value
0 1	ADD0 ADD1	A/D conversion result Bits 1 and 0 (LSB)	Indifinite
2	———	Unused	——
3	———	Unused	——

ADDM X 'C' R

bit	Name	Description	Initial Value
0 1 2 3	ADD2 ADD3 ADD4 ADD5	A/D conversion result Bits 5 to 2	Indifinite

ADDH X 'D' R

bit	Name	Description	Initial Value
0 1 2 3	ADD6 ADD7 ADD8 ADD9	A/D conversion result Bits 9 (MSB) to 6	Indifinite

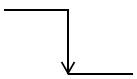
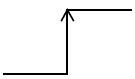
3.2.6 Interrupt Selection Registers

The interrupt selection registers are used for IRQ interrupt source selection, or the ON/OFF setting of each interrupt mask.

IRQC X 'F' R/W

bit	Name	Description	Initial Value
0	IRQSE0	IRQ interrupt source selection. See Note 1.	1
1	IRQSE1		1
2	MaskIR	Selects the IRQ interrupt masking. 1: Mask 0: Permit	1
3	IRQEC	Selects the IRQ interrupt edge. (See Note 1.) Refer to the following chart.	1

IRQSE0	IRQSE1	
0	0	Time base (See Note 2.)
0	1	Timer (See Note 3.)
1	0	ACZ (See Notes 4 and 5.)
1	1	$\overline{IRQ}$ (See Note 5.)

	Selection of IRQ enabled edge	
IRQEC set value	1	0
IRQ enabled edge		

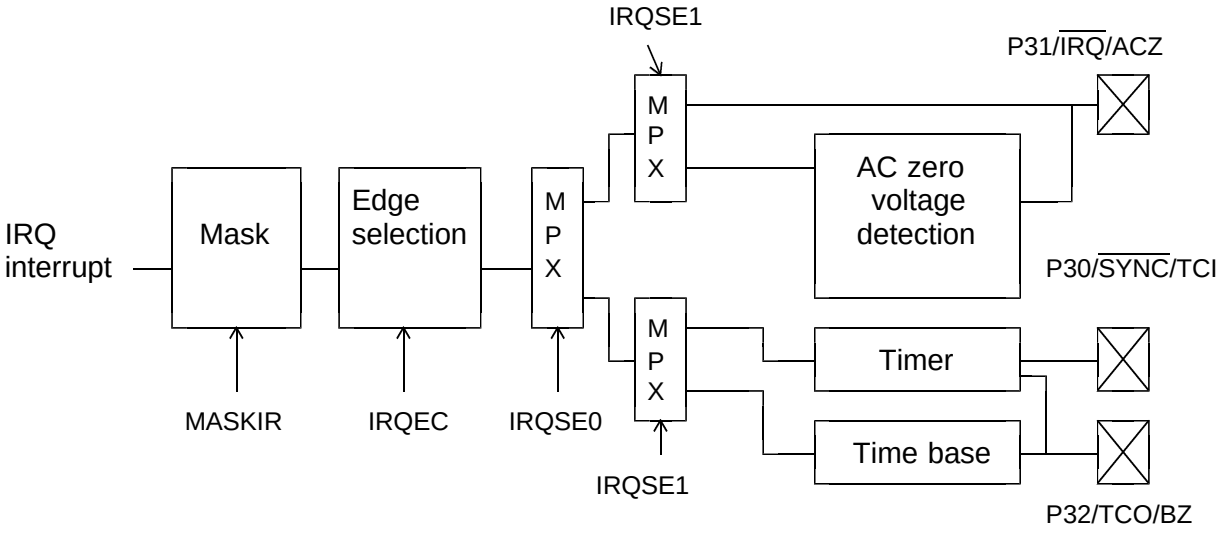
Note 1) Select the IRQ interrupt source or enabled edge after masking IRQ interrupt function with the MASKIR bit.

Note 2) Time base interrupt occurs at the rising or falling edge of buzzer output.

Note 3) Timer interrupt occurs in synchronization with a timer overflow. Therefore, no edge selection is enabled.

Note 4) If ACZ interrupt is selected, $\overline{IRQ}$ or P31 input is disabled.
ACZ interrupt occurs at the rising or falling edge of AC zero voltage detection output.
ACZ interrupt uses an edge trigger circuit. Therefore, more than one interrupt may occur due to chattering if the rising or falling time of the input signal is comparative long.
If the AC zero-cross is used, write an appropriate program for masking for the prevention of detection errors.

Note 5) The P31 output is set to Hi-Z if the $\overline{IRQ}$ or ACZ input is used as an IRQ interrupt source.



3.3 Available Instructions

The following instructions can access the I/O registers.

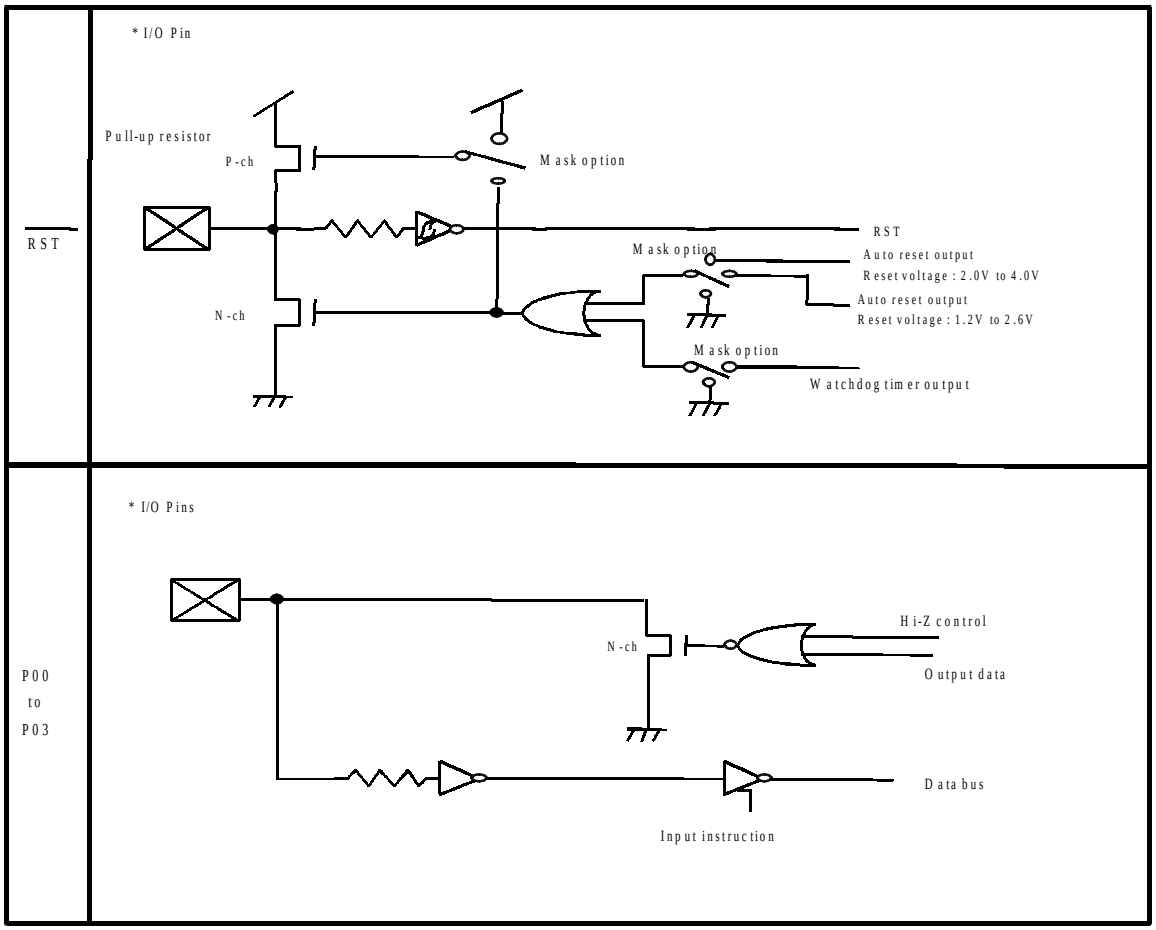
Addresses	Available Instructions
X '0' to X '4' X '7' to X 'A', X 'F'	IN, OUT
X 'B' to X 'D'	IN
X '5' to X '6' See Note 1.	IN, OUT

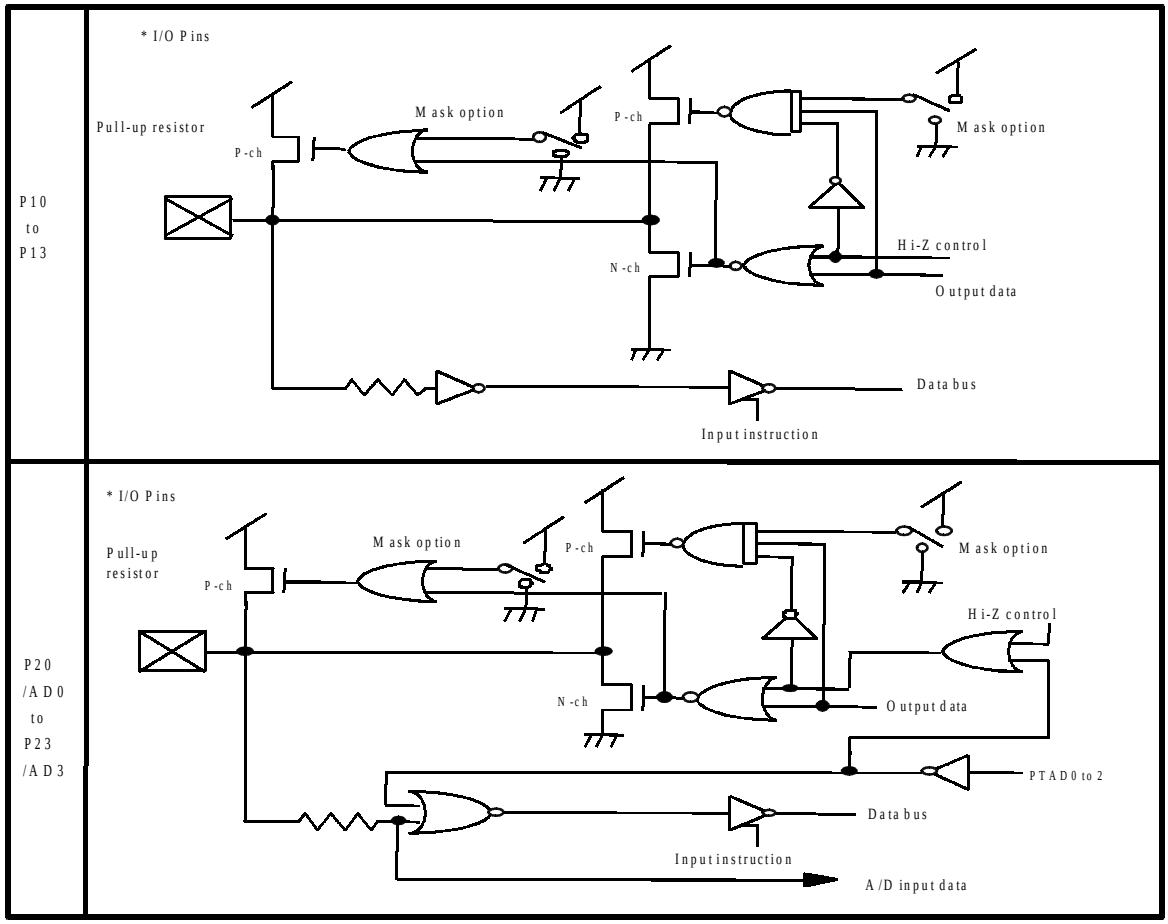
Note) The initial input of a register is indefinite and so is the input of the register while the LSI is in operation, if the register is not set up.

Note 1) The binary counter value is read when the IN instruction is executed.

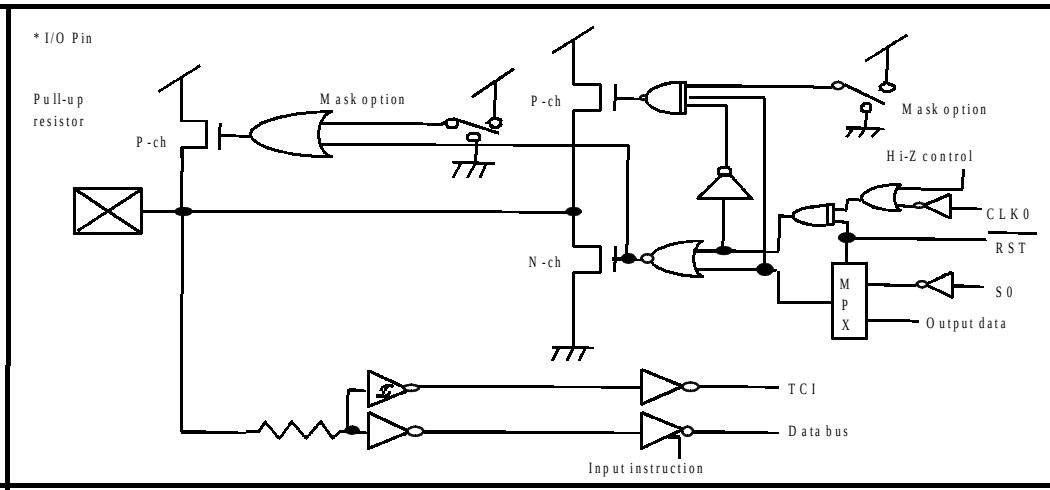
3.4 Pin Structure Diagram

The following shows the pin structure of this LSI.

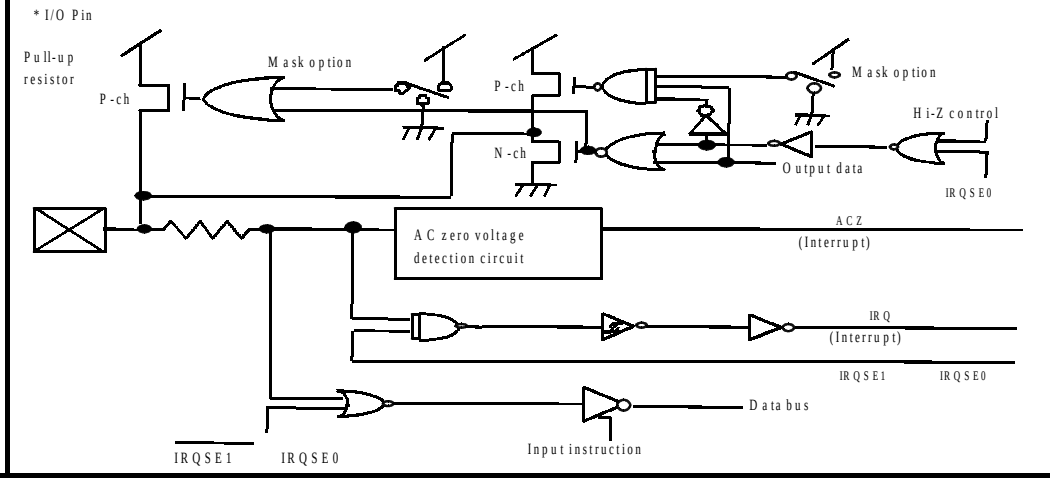


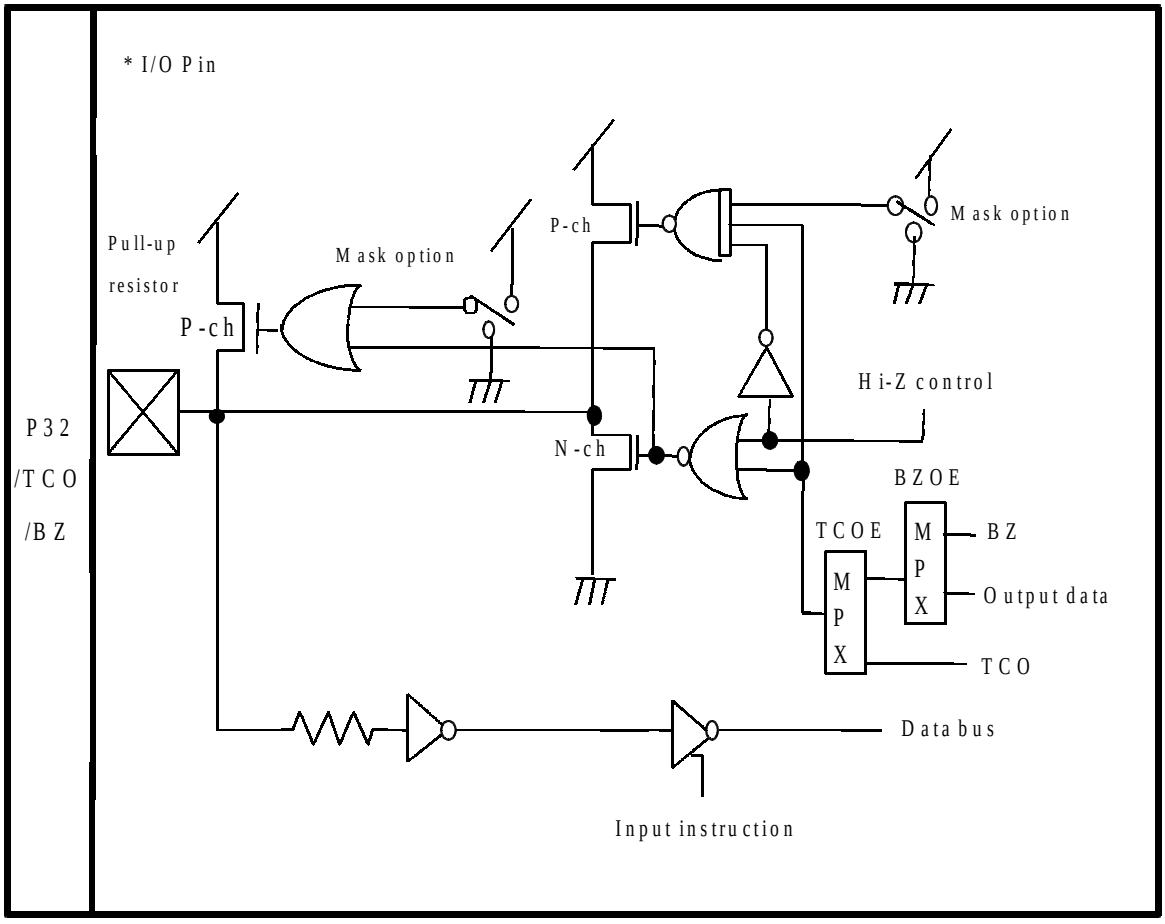

P10
to
P13
* I/O Pins
Pull-up resistor
P-ch
Mask option
P-ch
Mask option
Hi-Z control
N-ch
Output data
Data bus
Input instruction
P20
/AD0
to
P23
/AD3
* I/O Pins
Pull-up
resistor
P-ch
Mask option
P-ch
Mask option
Hi-Z control
N-ch
Output data
PTAD0 to 2
Data bus
Input instruction
A/D input data

P30
/SYNC
/TCI



P31
/IRQ
/ACZ




* I/O Pin
P32
/TCO
/BZ
Pull-up
resistor
P-ch
Mask option
P-ch
Mask option
Hi-Z control
N-ch
BZOE
TCOE
M
P
X
BZ
Output data
TCO
Data bus
Input instruction

CHAPTER 4 INTERRUPT FUNCTIONS

4.1 Interrupt Control

The interrupt control block breaks the flow of the running program with an interrupt request, saves the program status existing at break time to stack area, and controls the start of execution of an interrupt servicing program commensurate with each interrupt source. The user can use 4 kinds of interrupt sources except reset (These sources share the same first servicing address.) (See Fig. 4.1.1). With a JMP instruction, the first address of the interrupt servicing program can be freely specified from an interrupt start address (See Table 4.1.1).
An interrupt is received by the interrupt control block only when both the interrupt request flag (IF) and interrupt enable flag (IE) are set.
When an interrupt is received, the interrupt serving program starts running.
Table 4.1.2 shows an example of the interrupt enable/disable program.
The IRQ selects the source of interrupt and permits or prohibits the source through the IRQC (X'F').

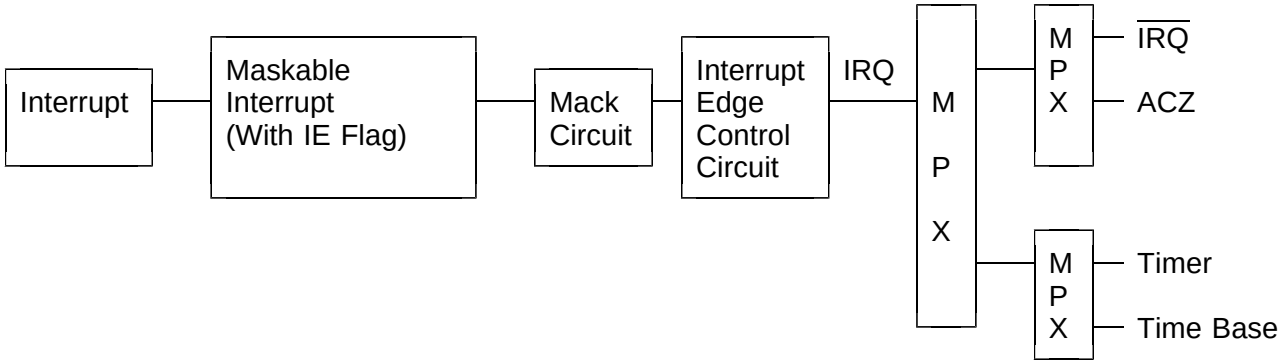


Fig. 4.1.1 Interrupt Sources

Table 4.1.1 Interrupt Servicing Program Start Address

Interrupt Source		Vector Address	Priority
(CPU reset)	(RESET)	000	↑ High
External signal interrupt	(IRQ)	00A	

Table 4.1.2 Example of Interrupt Setting Program

Setting Method	Enable	Disable
IRQ	EDI 0,4	EDI 4,0

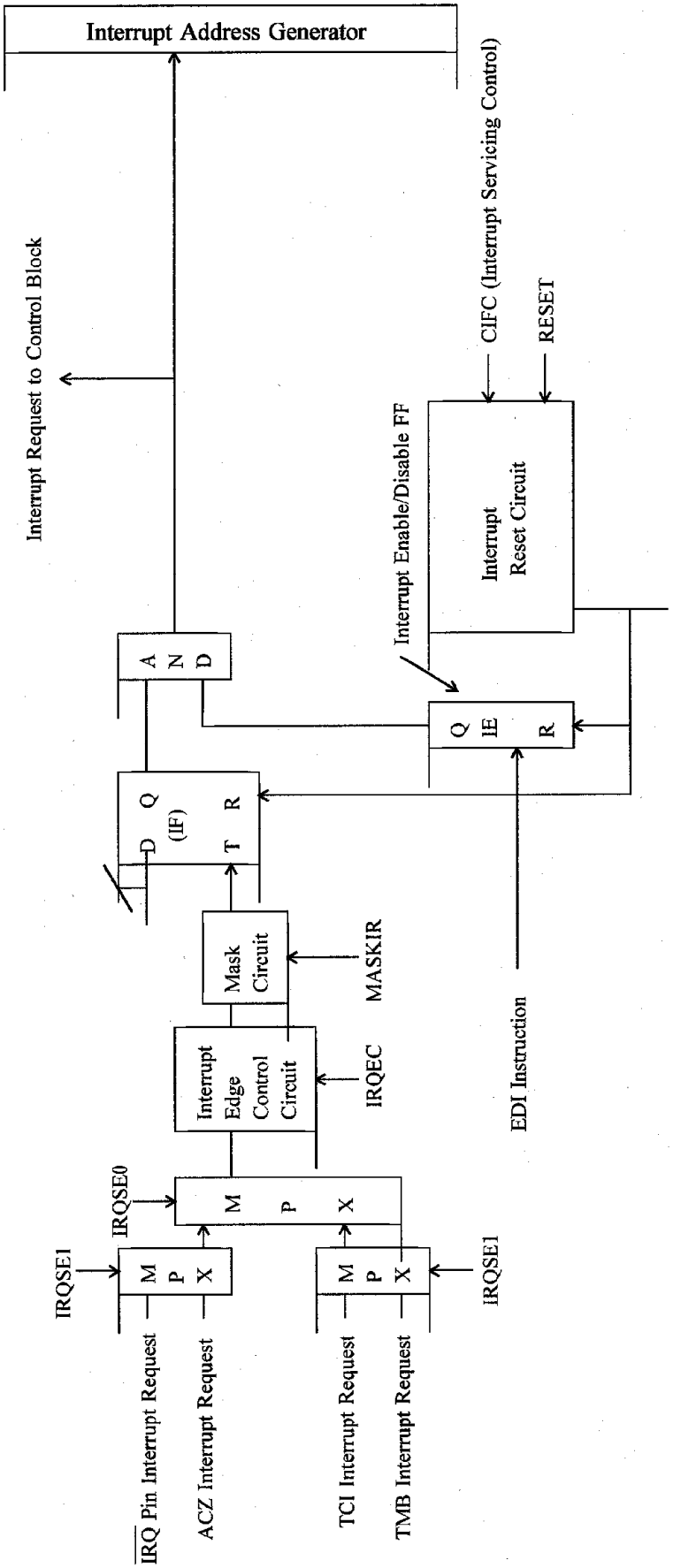
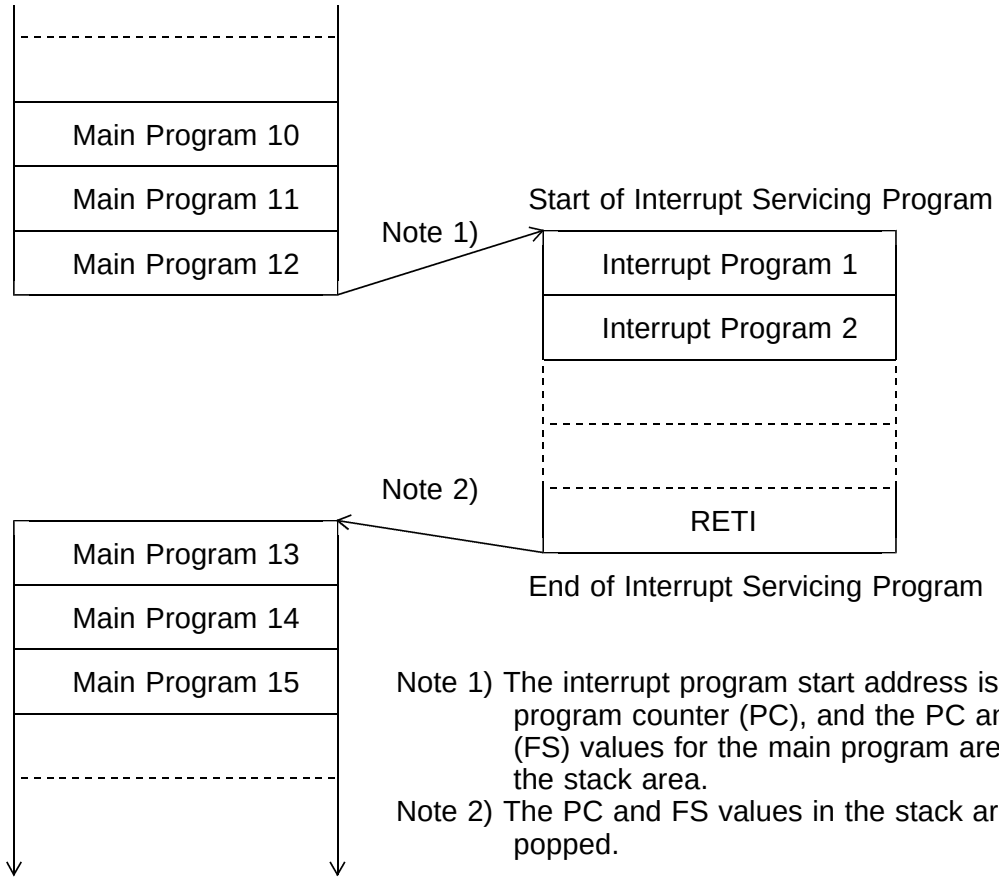


Fig. 4.1.2 Interrupt Block Diagram

4.2 Interrupt Receiving Operation

When an interrupt source such as timer is generated, the program is branched to the top of the interrupt servicing program to receive an interrupt (See Fig. 4.2.1). When an interrupt source is generated, the interrupt request flag (IF) is set.
When this is done, if the interrupt enable flag (IE) has been set, the generated interrupt source obtains the right to be received.
Interrupt reception functions similarly to when a CALL instruction is executed. In the interrupt reception cycle, the program counter (PC) and flag status (FS) are written (pushed) in the stack area RAM.
Next, the program counter (PC) is set in the specified interrupt servicing program start address. Then, the IE and IF are reset.
As desired, use the JMP instruction from the interrupt servicing program start address to run each interrupt servicing program.



Note 1) The interrupt program start address is set in the program counter (PC), and the PC and flag status (FS) values for the main program are pushed in the stack area.
Note 2) The PC and FS values in the stack area are popped.

Fig. 4.2.1 Interrupt Operation

The following shows an example of the interrupt servicing program.

Example) In case of IRQ

```
Absolute Address
    000A    JMP    LABEL

LABEL: PSHXY
       PSHEA

Interrupt Servicing Program

       POPEA
       POPXY
       EDI    0, 4
       RETI
```

4.3 Interrupt Return Operation

A RETI (Return from Interrupt) instruction is used to return from execution of the interrupt servicing program to the original program. The RETI instruction functions similarly to a RET (Return) instruction which is used to return from a subroutine to a main routine.
That is, by executing the RETI instruction, the values of the program counter (PC) and flag status (FS) just before an occurrence of an interrupt, pushed in the stack area RAM, are returned to the PC and FS, and the program flow existing before interrupt generation is restored.
It takes 4 machine cycles to start an interrupt servicing program after an interrupt source is generated. When there is an EDI instruction in the top address of the interrupt servicing program, the interrupt is disabled for 3 to 4 machine cycles.

4.4 Stack upon Interrupt

When receiving an interrupt or returning from it, the stack level changes by how much the program counter (PC) and flag status (FS) are pushed or popped.
In the case of a normal interrupt, the 4-word stack area RAM is required because the PC and FS are pushed. Therefore, the value of the stack pointer (SP) is decremented by 4 upon receiving the interrupt and incremented by 4 upon returning from the interrupt (See Fig. 4.4.1).
A return from interrupt is done by executing the RETI instruction. The RETI instruction restores the original values of the FS and PC which have been pushed in the stack area RAM during the interrupt reception cycle. The SP is incremented after reading out the values in the RAM indicated by SP.

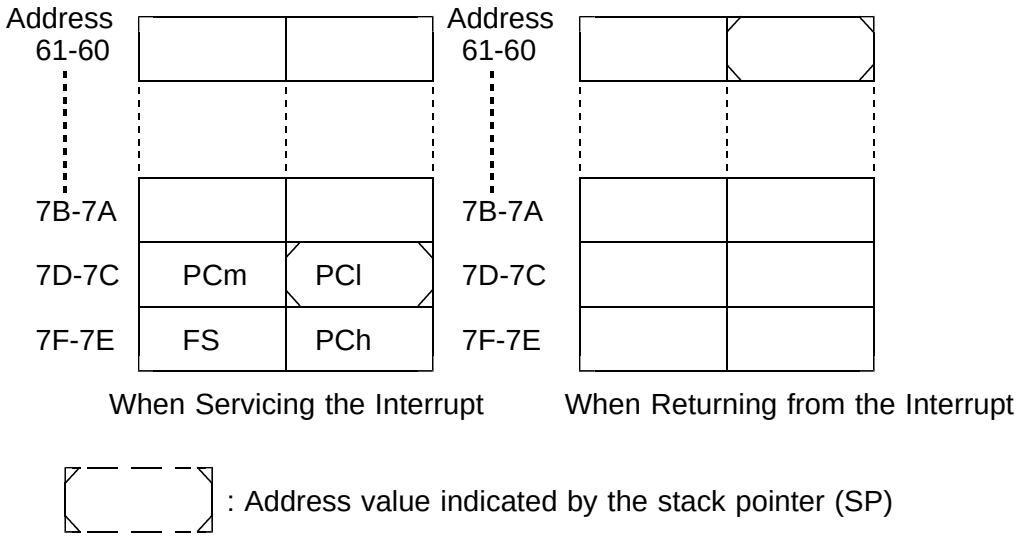


Fig. 4.4.1 Stack Pointer Operation

CHAPTER 5 TIMER FUNCTION

As shown in Fig. 5.1.1, this LSI incorporates an 8-bit timer/counter and operates in timer mode or event count mode.
To start the timer, execute the OUT instruction to set the desired time value in the timer buffer (TB) first and set the clock source in the timer control register (TM) next. Then the value in the timer buffer (TB) is transferred to the binary counter (BC) and the clock selected with the TM starts counting.
When the BC overflows, the interrupt reception flag (IF) is set and the TB value is set again in the BC simultaneously, provided that the interrupt source of IRQ has been selected for the timer with software with the mask option cleared. The BC repeats the above-mentioned sequence unless the control mode is changed.

1. Timer Mode
   In timer mode, one of the following clocks is selected by the TM and the BC uses the one selected by the TM to start counting.
   (1) 1/2 f_{sys} (f_{sys}: internal clock)
   (2) $1/2^{14}$ of OSC1 pin input pulse frequency

2. Event Count Mode
   In event count mode, one of the following clocks is selected by the TM and the BC uses the one selected by the TM to start counting.
   (1) TCI pin input pulse as it is
   (2) $1/2^{6}$ of TCI pin input pulse frequency
   Refer to the specifications of external clock input 3 for the waveform of TCI input.
   P30 output is set to Hi-Z in event count mode with TCI input selected.

Note) The BC value cannot be read at a single time but in the order of the upper bits and lower bits. Pay utmost attention to and take into consideration the timing that the BC value changes while reading it.

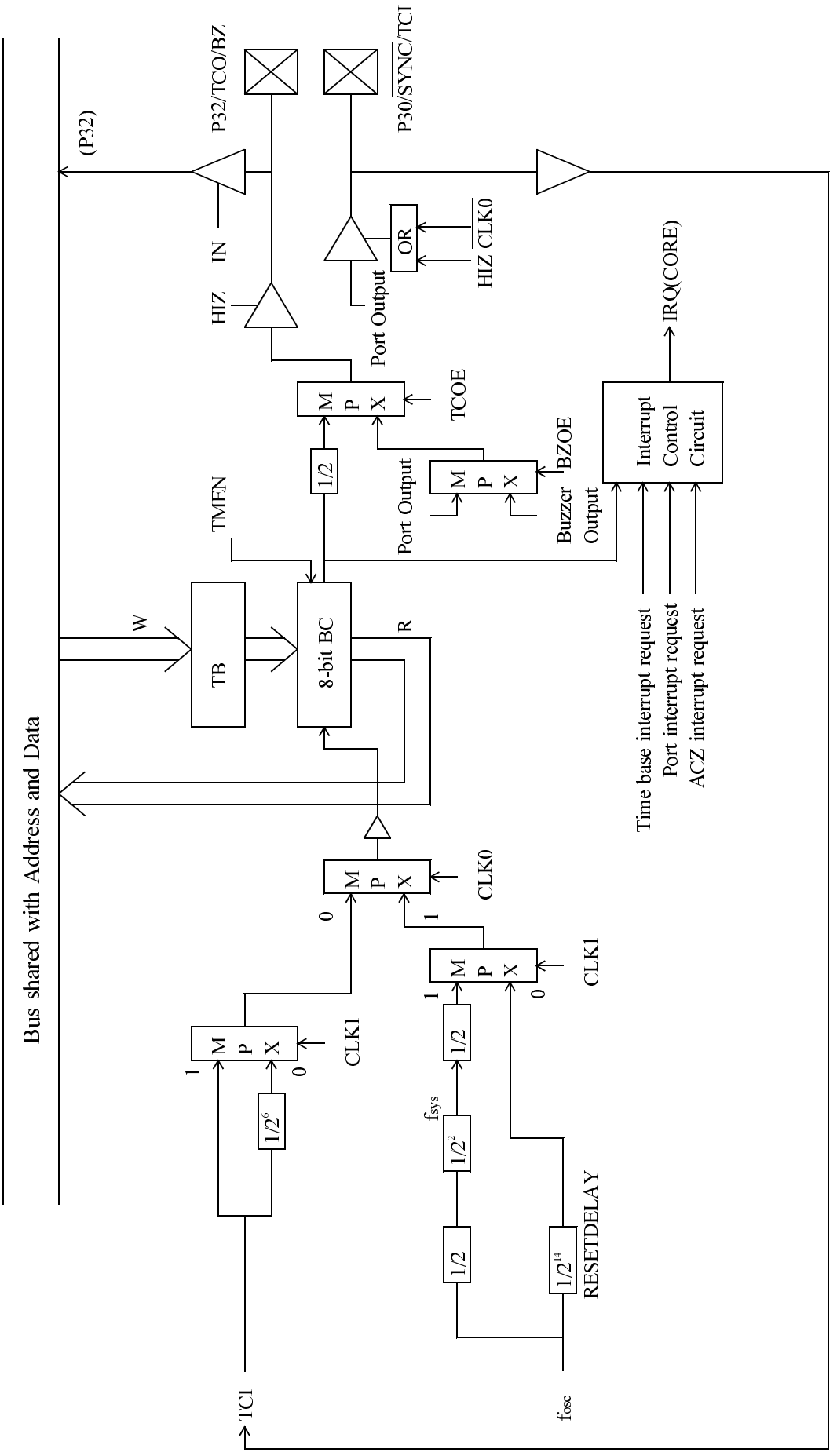


Fig. 5.1.1 Timer Function Operation Block Diagram

1) The following shows the bit allocation of the timer control register (TM).

TM X '7' R/W

<table>
<tr><th>bit</th><th>Name</th><th>Description</th><th>Initial Value</th></tr>
<tr><td>0</td><td>TMEN</td><td>Specifies timer operation.
1: The timer stops
0: The timer operates</td><td>1</td></tr>
<tr><td>1</td><td>TCOE</td><td>Selects P32, TCO or BZ.
(Selects port I/O, timer output or buzzer output.)
1: Selects P32/BZ (port I/O or buzzer output)
0: Selects TCO (timer output)
Note) Select P32 or BZ with bit 1 (BZOE) of the X '8' port register.</td><td>1</td></tr>
<tr><td>2</td><td>CLK0</td><td rowspan="2">Selects the clock of timer.
<table>
<tr><th>CLK0</th><th>CLK1</th><th>Clock Source</th></tr>
<tr><td>0</td><td>0</td><td>TCI input/2^6
See Note 1.</td></tr>
<tr><td>0</td><td>1</td><td>TCI input
See Note 1.</td></tr>
<tr><td>1</td><td>0</td><td>$f_{osc}/2^{14}$</td></tr>
<tr><td>1</td><td>1</td><td>f_{sys} /2
See Notes 2 and 3.</td></tr>
</table></td><td>1</td></tr>
<tr><td>3</td><td>CLK1</td><td>1</td></tr>
</table>

Note 1) The P30/$\overline{\text{SYNC}}$/TCI output is set to Hi-Z.
Note 2) f_{sys} = 1/8 f_{osc}.
Note 3) If $f_{sys}/2$ is selected, the timer stops when the LSI is in HALT mode.

2) Timer buffer (TB) setting method

A timer buffer (TB) set value is obtained by the following expression.
Set value = 256 - Desired counts
(1 ≦ Desired counts ≦ 256)
Example 1) Timer buffer (TB) set value when counting 100 times
Set value = 256 - 100
= 156
= 9C (hex)

5.1 Description of Timer Function

Application	Mode	Timer Mode Registers		TB Set Value	Output Frequency
		CLK1	CLK0		
Clock	Timer mode (f_{osc}=4.19 MHz)	0	1	80 C0 E0 F0	1 Hz(1s) 2 Hz(0.5 s) 4 Hz(0.25 s) 8 Hz(0.125 s)
	Event mode (f_{tci}=32.768 kHz)	0	0	00 80 C0 E0	1 Hz 2 Hz 4 Hz 8 Hz
BZ	Timer mode (f_{osc}=4.19 MHz)	1	1	80 C0	1.024 kHz 2.048 kHz
	Timer mode (f_{osc}=4.0 MHz)	1	1	80 C0	0.976 kHz 1.953 kHz
	Event mode (f_{tci}=32.768 kHz)	1	0	F0 F8	1.024 kHz 2.048 kHz
Melody	Timer mode (f_{osc}=4.0 MHz)	1	1	Table 7.2.1 Melody frequencies (example)	

Sound	n*	TB set value	Output frequency (Hz)	Temperament scale (Hz)
C7 Do	60	C4	2083.3	2093
C7	57	C7	2192.9	2217
D7 Re	54	CA	2314.8	2349.3
D7	51	CD	2451	2489
E7 Mi	48	D0	2604.2	2637
F7 Fa	45	D3	2777.8	2793.8
F7	43	D5	2907	2960
G7 So	40	D8	3125	3136
G7	38	DA	3289.5	3322
A7 La	36	DC	3472.5	3520
A7	34	DE	3676.5	3729
B7 Si	32	E0	3906.3	3351.1
C8 Do	30	E2	4166.7	4186

*n = number of desired counts

CHAPTER 6 TIME BASE FUNCTION

As shown in Fig. 6.1.1, this LSI has a function to output clock signals that are generated by dividing the frequency of oscillation source to the pin or accumulator. Furthermore, by selecting time base interrupt with the IRQC in software control, the output can be used as an interrupt source. Right after the P32/TCO/BZ pin is set to buzzer output, the initial buzzer output value, the period until the first output signal's rising edge, or the period until the signal's falling edge is indefinite or not guaranteed.
The following table shows the bit allocations of the time base control register (TMBC).

TMBC X '8' R/W (Bit 0 is read-only)

<table>
<tr><th>bit</th><th>Name</th><th>Description</th><th>Initial Value</th></tr>
<tr><td>0</td><td>TMB</td><td>When the IN instruction is executed, the clock value, which is obtained by dividing the frequency of oscillation source by the BZSEL0 signal and BZSEL1 signal, is set in bit 0 of the accumulator.</td><td>Indefinite</td></tr>
<tr><td>1</td><td>BZOE</td><td>Selects P32, TCO or BZ.
1: Selects P32
0: Selects BZ (buzzer output)
Note) The setting in the BZOE bit is disabled if TCO output is selected with the TCOE bit.</td><td>1</td></tr>
<tr><td>2</td><td>BZSEL0</td><td rowspan="2">Selects clock output to be provided to the buzzer and time base.
<table>
<tr><th>BZSEL0</th><th>BZSEL1</th><th>Clock Source</th></tr>
<tr><td>1</td><td>1</td><td>fosc/2^{12}</td></tr>
<tr><td>1</td><td>0</td><td>fosc/2^{11}</td></tr>
<tr><td>0</td><td>1</td><td>fosc/2^{10}</td></tr>
<tr><td>0</td><td>0</td><td>fosc/2^{9}</td></tr>
</table></td><td>1</td></tr>
<tr><td>3</td><td>BZSEL1</td><td>1</td></tr>
</table>

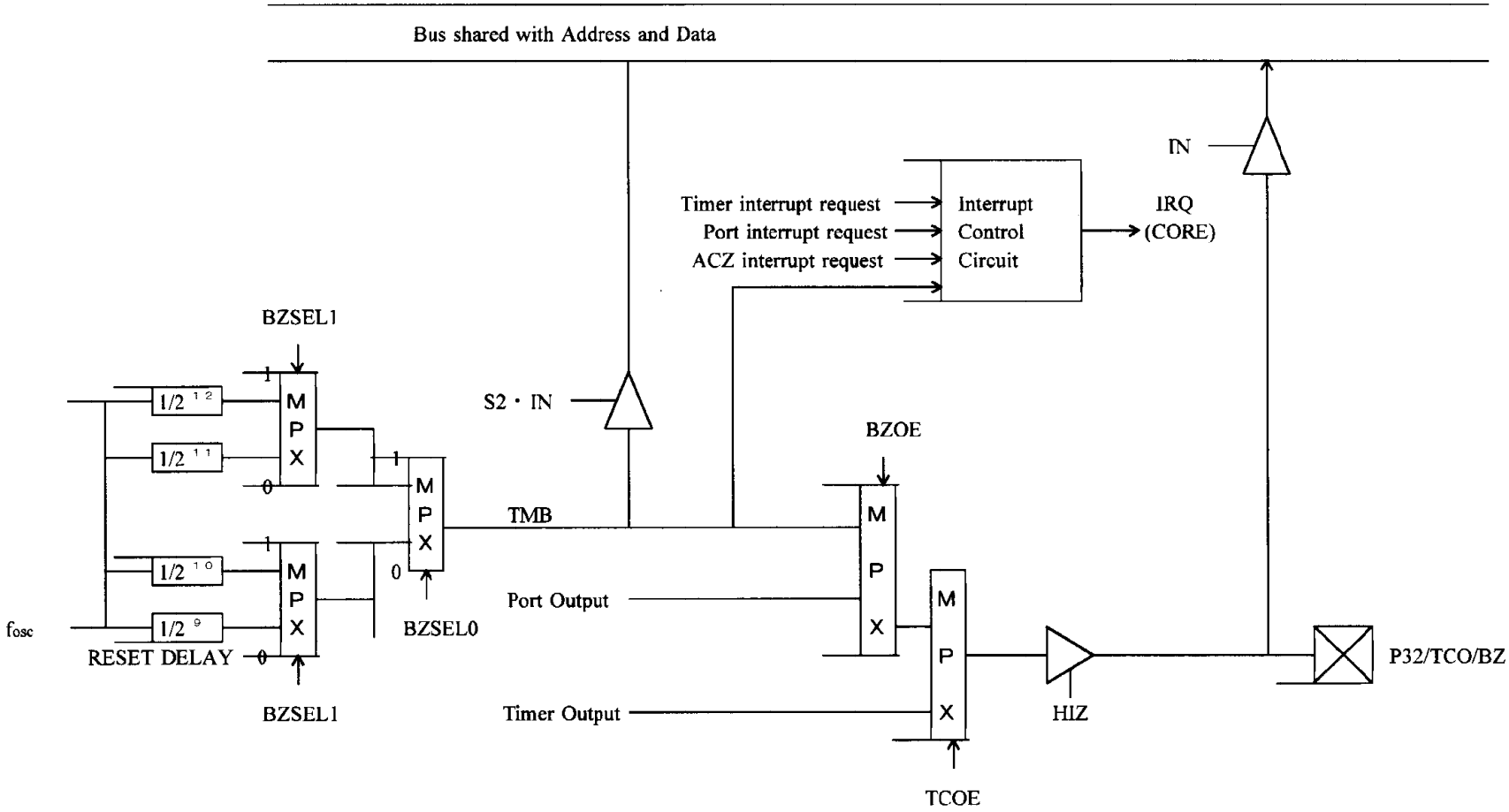


Fig. 6.1.1 Time Base Function Operation Block Diagram

CHAPTER 7 A/D CONVERSION FUNCTION

7.1 Overview

This LSI incorporates a 10-bit A/D converter and sample-and-hold circuit.

7.2 A/D Conversion Function

Fig. 7.2.1 shows a block diagram of the A/D converter. The analog input between the V_{DD} and V_{SS} voltages are divided by 1024 to convert the analog input into digital values. Therefore, V_{IN} voltage input into the P20/AD0 to P23/AD3 pins is converted into digital values for X '3FF' to X '000' on condition that the voltage V_{IN} is within a range between the voltages V_{SS} and V_{DD}. ($V_{DD} \geqq V_{IN} \geqq V_{SS}$)
A/D conversion starts with channel selection, followed by the start control of A/D conversion through the A/D control register (ADC).
The A/D conversion result is set in the A/D buffer (ADD).
In A/D conversion operation, sampling is performed for the Ts period. Then if the conversion result with its MSB set to 1 is larger than 1/2 V_{DD}, (1/2 + 1/4) V_{DD} is compared with the voltage V_{IN} with both MSB and the second most significant bit set to 1. If the voltage V_{IN} is smaller than 1/2 V_{DD}, 1/4 V_{DD} is compared with the voltage V_{IN} with MSB set to 0 and the second most significant bit set to 1. Value comparison with the voltage V_{IN} is repeated 10 times in sequence in this way to complete A/D conversion.
Provided that the A/D conversion reference clock cycle, T_{AD}, is 1 ms at 8 MHz (i.e., 1/8 f_{osc}), the whole A/D conversion period is 15 µs, that is, 15×T_{AD} (1 µs).
If the impedance of the analog signal to be converted is high, drop the conversion speed by setting the ADTC of the A/D control register (ADCH) to zero. In that case, it takes 27 µs (i.e., 27×T_{AD}) to complete A/D conversion, provided that the T_{AD} is 1 ms at 8 MHz (i.e., 1/8 f_{osc}). Refer to Fig. 7.2.2.

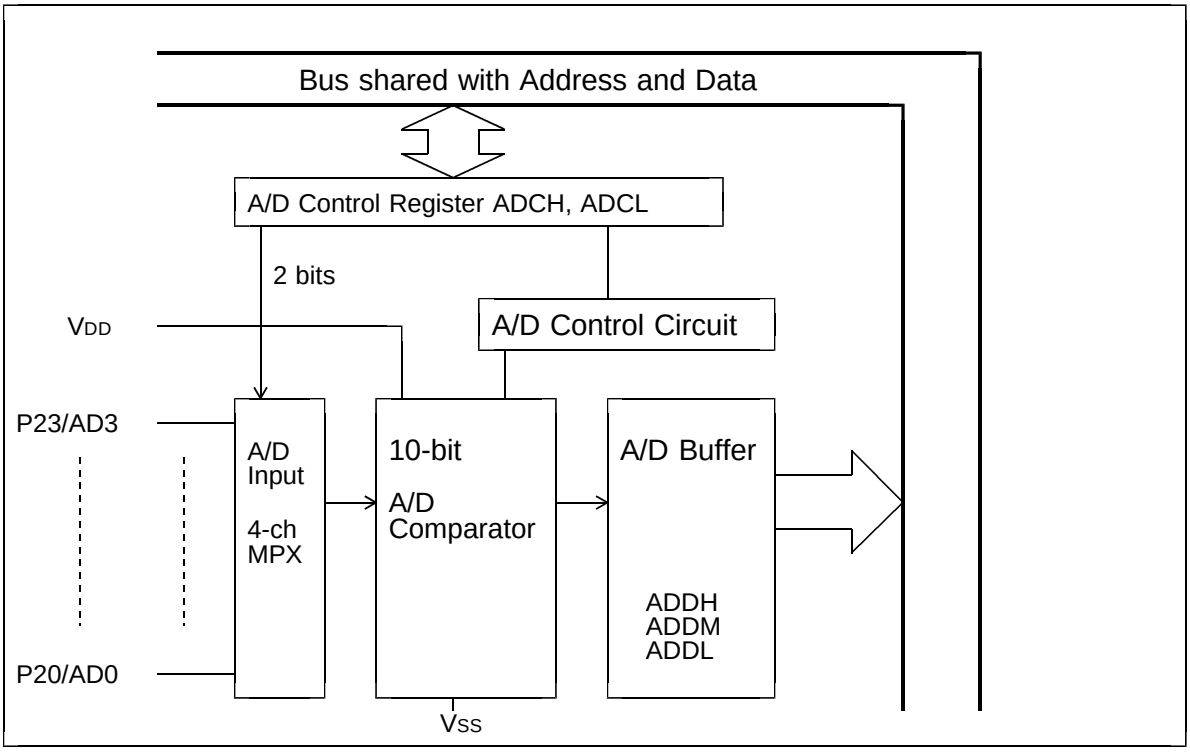
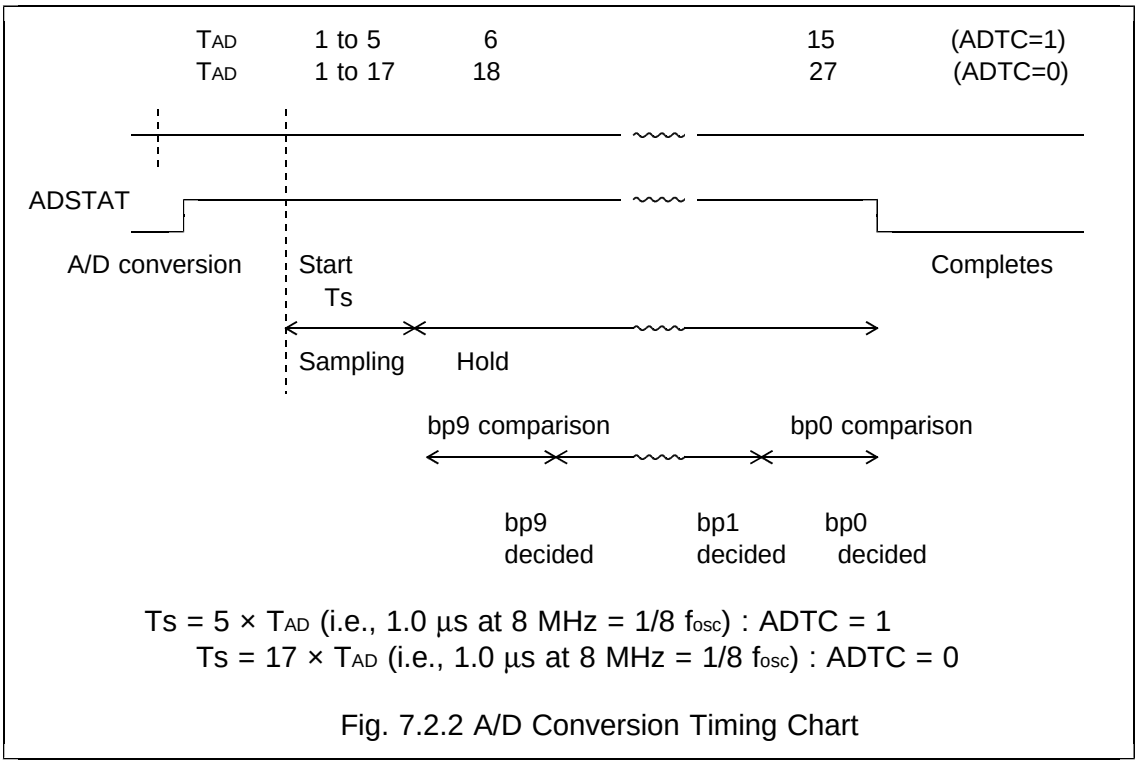


Fig. 7.2.1 A/D Conversion Control Circuit Block Diagram



Ts = 5 × T_{AD} (i.e., 1.0 µs at 8 MHz = 1/8 f_{osc}) : ADTC = 1
Ts = 17 × T_{AD} (i.e., 1.0 µs at 8 MHz = 1/8 f_{osc}) : ADTC = 0

Fig. 7.2.2 A/D Conversion Timing Chart

As shown in Fig. 7.2.3, this A/D converter is of capacitor array construction. Right after the start of the conversion of an analog signal, a change in the voltage of the analog signal may result if the impedance of the analog signal to be converted is high.
In order to ensure the accuracy of A/D conversion, be sure to use the microcomputer under the following conditions, otherwise proper A/D conversion cannot be guaranteed.

(1) The recommendable impedance of the analog signal to be converted is 100 kΩ maximum and the signal is input into the A/D input pin through a minimum capacitance of 500 pF. One of the following condition is also required according to the impedance.
100 k W max. : A minimum conversion time of 27 µs is required.
100 kΩ to 400 kΩ : A minimum conversion time of 50 µs is required.
400 k Ω min. : Input the analog signal through a capacitor of minimum 1000 pF.

(2) For the prevention of the fluctuation of the power supply voltage during A/D conversion, do not change the output level of the microcomputer to low from high or vice versa or turn the peripheral load circuit on or off.

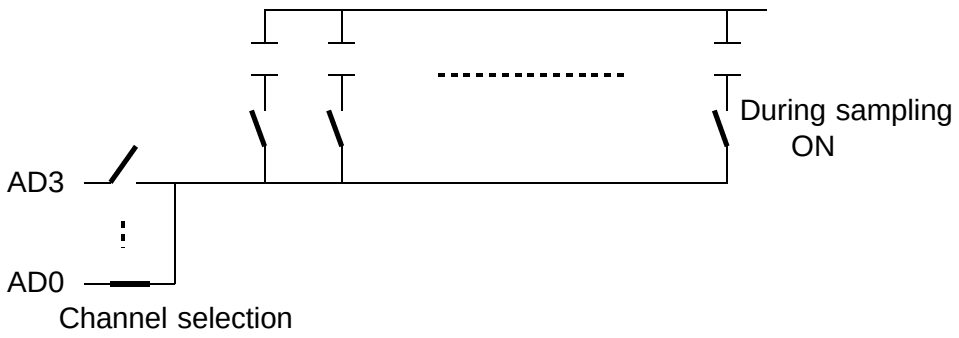


Fig. 7.2.3 A/D Input Equivalent Circuit

7.3 Functional Registers of A/D Converter

The A/D converter incorporates the A/D control register (ADC) and A/D buffer (ADD). The ADC controls A/D conversion and the ADD stores the result of A/D conversion.

7.4 A/D Buffer

The A/D buffer is a 4-bit, read-only register that is allocated to the addresses X 'B', X 'C' and X 'D' in the RAM.

ADDL X 'B' R

bit	Name	Description	Initial Value
0 1	ADD0 ADD1	A/D conversion result Bits 1 and 0 (LSB)	Indifinite
2	———	Unused	———
3	———	Unused	———

ADDM X 'C' R

bit	Name	Description	Initial Value
0 1 2 3	ADD2 ADD3 ADD4 ADD5	A/D conversion result Bits 5 to 2	Indifinite

ADDH X 'D' R

bit	Name	Description	Initial Value
0 1 2 3	ADD6 ADD7 ADD8 ADD9	A/D conversion result Bits 9 (MSB) to 6	Indifinite

7.5 A/D Control Register

This is a 4-bit read/write register that is allocated to the addresses X '9' and X 'A' of port register.

ADCL X '9' R/W

<table>
<tr><th>bit</th><th>Name</th><th>Description</th><th>Initial Value</th></tr>
<tr><td>0</td><td>ADCHS0</td><td rowspan="4">Selects the channel for A/D conversion.
<table><tr><th>ADCHS0</th><th>ADCHS1</th><th>Channel</th></tr><tr><td>1</td><td>1</td><td>AD0</td></tr><tr><td>1</td><td>0</td><td>AD1</td></tr><tr><td>0</td><td>1</td><td>AD2</td></tr><tr><td>0</td><td>0</td><td>AD3</td></tr></table></td><td>1</td></tr>
<tr><td>1</td><td>ADCHS1</td><td>1</td></tr>
<tr><td>2</td><td>ADSTAT</td><td>Indicates the operation status of A/D conversion.
1: A/D conversion is completed or is not in process.
0: A/D conversion has started or is in process.</td><td>1</td></tr>
<tr><td>3</td><td>ADTC</td><td>Selects the A/D conversion rate.
1: 15 machine cycles
0: 27 machine cycles</td><td>1</td></tr>
</table>

ADCH X 'A' R/W

<table>
<tr><th>bit</th><th>Name</th><th>Description</th><th>Initial Value</th></tr>
<tr><td>0</td><td>PTAD0</td><td rowspan="3">Selects P20 to P23 or AD0 to AD3 signals.
<table><tr><th>PTAD0</th><th>PTAD1</th><th>PTAD2</th><th>Setting</th></tr><tr><td>0</td><td>0</td><td>0</td><td>Selects AD0 to AD3</td></tr><tr><td>1</td><td>0</td><td>0</td><td>Selects AD0 to AD2 and P23</td></tr><tr><td>0</td><td>1</td><td>0</td><td>Selects AD0, AD1, P22 and P23</td></tr><tr><td>1</td><td>1</td><td>0</td><td>Selects AD0 and P21 to P23</td></tr><tr><td>*</td><td>*</td><td>1</td><td>Selects P20 to P23</td></tr></table>* : Don't care</td><td>1</td></tr>
<tr><td>1</td><td>PTAD1</td><td>1</td></tr>
<tr><td>2</td><td>PTAD2</td><td>1</td></tr>
<tr><td>3</td><td>ADHAL</td><td>Disconnects the reference power supply in order to save the current consumption of the A/D converter.
1: A/D converter not in use.
0: A/D converter in use.</td><td>1</td></tr>
</table>

Note) When the A/D converter is in use, set the analog data input pins to analog data input only mode. On that occasion, the pin which selects AD cannot be connented to a pull-up resister. To set the LSI to low-current consumption mode (i.e., STOP or HALT mode), set the ADHALT bit to 1.

CHAPTER 8 AC ZERO VOLTAGE DETECTION FUNCTION

The ACZ pin is the input pin of the AC zero voltage detection circuit.
The AC zero voltage detection circuit usually has low-level output, but when the input level is middle, the circuit has high-level output.
The ACZ input signal shares the pin with the P31 and $\overline{IRQ}$ interrupt input signals.
It is possible to select the output of the AC zero voltage detection circuit, timer output, time base output or the $\overline{IRQ}$ pin as an IRQ interrupt source with software. Refer to Interrupt Selection Register for details.
An input clamp diode is connected to the ACZ input circuit.

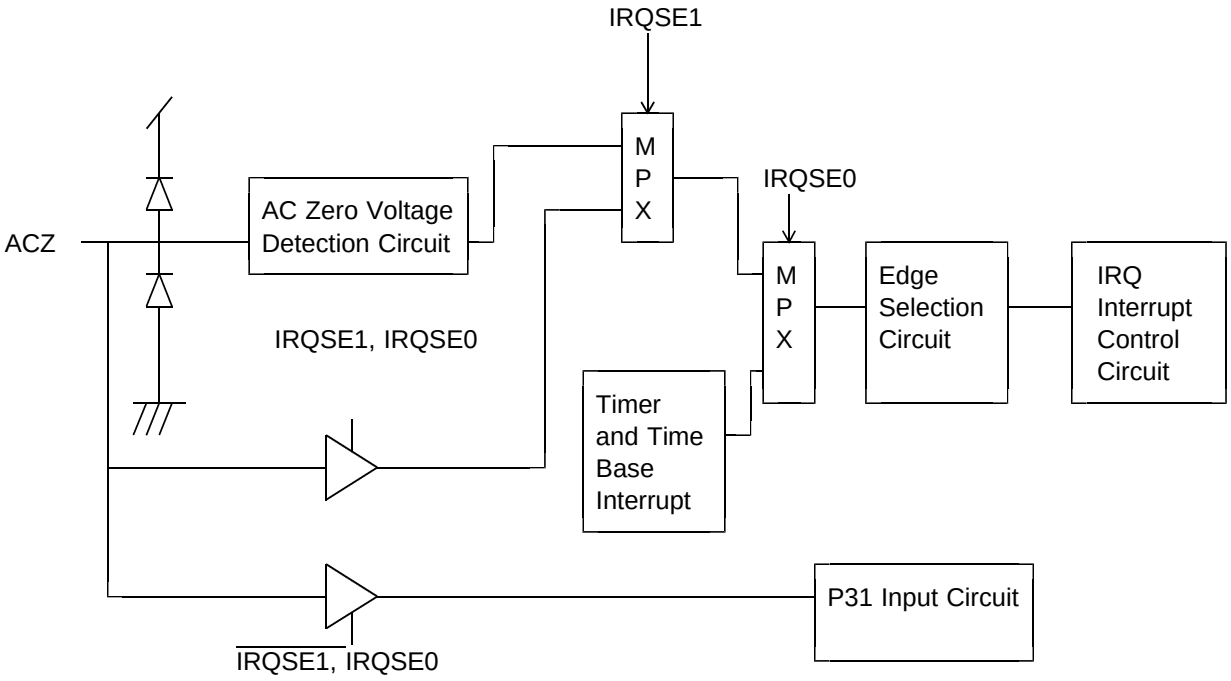


Fig. 8.1.1 AC Zero Voltage Detection Circuit Block Diagram

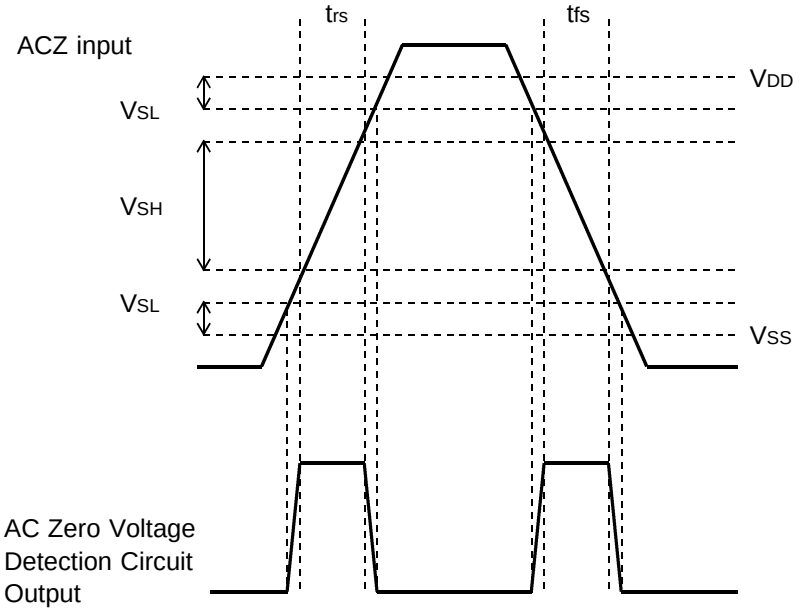


Fig. 8.1.2 Timing Chart

CHAPTER 9 WATCHDOG TIMER FUNCTION

This LSI has a function to divide the frequency of oscillation source and turns on the low-level output of the reset pin when an overflow occurs. This function is selectable as a mask option. The watchdog timer starts when the internal reset status of the CPU is cleared while the LSI awaits the stabilization of OSC oscillation after the LSI is turned on or reset.
By setting the WDEN bit of the CPU control register (CPUM X '4') to 1 before an overflow of the divide-by-2^6 counter, the divide-by-2^6 counter is cleared. After clearing, the counter starts operating again.
The counter of the watchdog timer overflows within a range between 32256 and 32768 machine cycles after the counter is cleared.

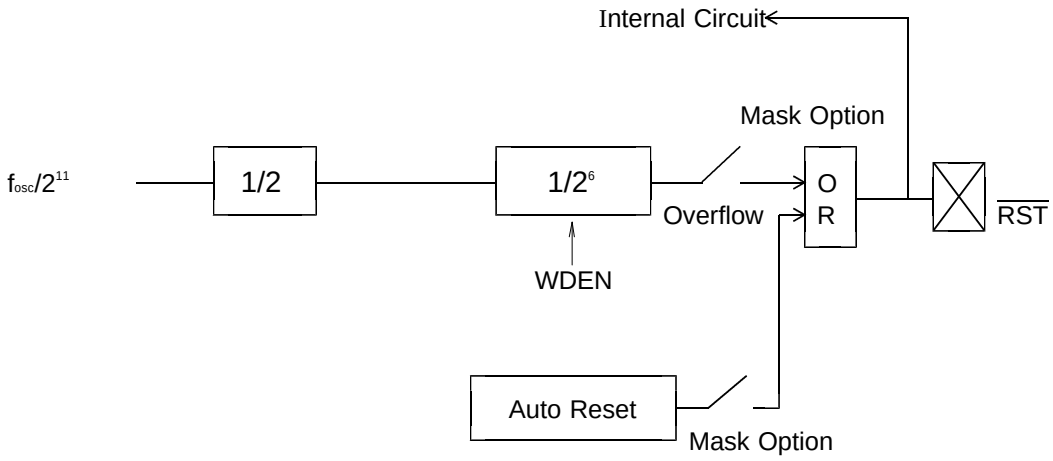


Fig. 9.1.1 Watchdog Timer

CPUM X '4' R/W(Bit 1 is write-only.)

bit	Name	Description	Initial Value
0	HIZC	Sets the Hi-Z of all output pins. (See Note 1.)	1
1	WDEN	Clears or enables the watchdog timer. (See Note 2.) 1: Cleared 0: Enabled	0
2	——	Always set to 1.	1
3	——	Not used.	——

Note 1) The $\overline{\text{SYNC}}$ pin and the pull-up selection pins are excluded from Hi-Z control.
Note 2) The watchdog timer restarts after the watchdog timer is cleared with the WDEN bit set to 1, provided that the watchdog timer is selected as a mask option.

For further details on the instruction sets, please refer to the Instruction Manual/the MN1500 Series User's Manual.

MN150222 Instruction Sets List

M \ L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP		CPL ZF	RC CF				SC CF	ROL ZF CF							C ZF CF
1		AC ZF CF		SB ZF CF	O ZF	X ZF	N ZF	L ZF								LD ZF
2	ICY ZF	LICY ZF	STICY ZF		DCY ZF											
3					RET	RETI ZF CF			RBMD ZF				SBMD ZF			
4					LX ZF	LY ZF		EX			WI					
5				STD	STX	STY		ST				EDI				
6	ICM ZF CF				DCM ZF CF				PSHEA	PSHXY	JNZ	JNC	POPEA	POPXY	JZ	JC
7			OUT	IN					JBZ				JBNZ			
8																
9	CALL															
A	JMP															
B	CYIJ ZF															
C	LYI															
D	AI ZF CF															
E	CI ZF CF															
F	LI															

ZF CF Affected flag

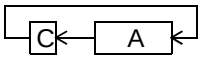
1-byte 1-cycle instruction

1-byte 2-cycle instruction

2-byte 2-cycle instruction

INSTRUCTIONS LIST

∧:Logical Product (AND) ∨:Logical Sum (OR) ":Exclusive Logical Sum (XOR)

	Instruction		InstructionCode (HEX)	Affected Flag	Operation
Transfer Instructions	L		17	ZF	A ← M(X,Y)
	LD	**	1F,da	ZF	A ← M(da)
	LX	LY	44	ZF	A ← X
			45	ZF	A ← Y
	LI		Fn		A ← n
	LICY	*	21	ZF	A ← M(X,Y) ; Y ← Y + 1
	ST		57		M(X,Y) ← A
	STD	**	53,da		M(da) ← A
	STX		54		X ← A
	STY		55		Y ← A
	STICY	*	22	ZF	M(X,Y) ← A ; Y ← Y + 1
	EX		47		A ↔ M(X,Y)
	LYI		Cn		Y ← n
	PSHEA		68		SP ← SP - 1;M(SP) ← A
					SP ← SP - 1
	POPEA		6C		SP ← SP + 1
					A ← M(SP);SP ← SP + 1
	PSHXY		69		SP ← SP - 1;M(SP) ← X
					SP ← SP - 1;M(SP) ← Y
	POPXY		6D		Y ← M(SP) ; SP ← SP + 1
					X ← M(SP) ; SP ← SP + 1
Operational Instruction	AI		Dn	CF,ZF	A ← A + n
	AC		11	CF,ZF	A ← A + M(X,Y) + CF
	SB		13	CF,ZF	A ← A - M(X,Y) - CF
	O		14	ZF	A ← A ∨ M(X,Y)
	X		15	ZF	A ← A "M(X,Y)
	N		16	ZF	A ← A ∧ M(X,Y)
	C		0F	CF,ZF	A — M(X,Y) (A unchanged)
	CI		En	CF,ZF	A — n (A unchanged)
	ICM		60	CF,ZF	M(X,Y) ← M(X,Y) + 1
	DCM		64	CF,ZF	M(X,Y) ← M(X,Y) - 1
	ICY		20	ZF	Y ← Y + 1
	DCY		24	ZF	Y ← Y - 1
	CPL		02	ZF	A ← $\overline{A}$
	ROL		08	CF,ZF	
	RBMD	**	3(8+b),da	ZF	M(da;b) 0
	SBMD	**	3(C+b),da	ZF	M(da;b) 1

	Instruction		Instruction Code (HEX)	Affected Flag	Operation
I/O Instructions	IN	**	73,pn		A ← PORT(p) ∧ n
	OUT	**	72,pn		PORT(p) ← A ∧ n
Control Instructions	NOP		00		
	WI		4A		
	RC		03	CF	CF ← 0
	SC		07	CF	CF ← 1
	JMP	**	Ah,ml		PC ← hml
	EDI	**	5B,mn		IE ← IE ∧ $\overline{m}$ ∨ n
	CALL	**	9h,ml		SP ← SP - 2 M(SP) ← PC ; PC ← hml
	RET	*	34		PC ← M(SP) ; SP ← SP + 2
	RETI	*	35	CF,ZF	CF/ZF/PC ← M(SP) ; SP ← SP + 2
	JBZ	**	7(8+b),ml		if A(b) = 0 then PCm/l ← ml else PC ← PC + 2
	JBNZ	**	7(C+b),ml		if A(b) = 1 then PCm/l ← ml else PC ← PC + 2
	JZ	**	6E,ml		if ZF = 1 then PCm/l ← ml else PC ← PC + 2
	JNZ	**	6A,ml		if ZF = 0 then PCm/l ← ml else PC ← PC + 2
	JC	**	6F,ml		if CF = 1 then PCm/l ← ml else PC ← PC + 2
	JNC	**	6B,ml		if CF = 0 then PCm/l ← ml else PC ← PC + 2
	CYIJ	**	Bn,ml	ZF	if Y = n then PC ← PC + 2 else PCm/l ← ml

* 1-byte 2-cycle instruction (1 ROM byte used, 2.0-ms execution time (f_{osc}=8 MHz,1/8 f_{osc}))
** 2-byte 2-cycle instruction (2 ROM byte used, 2.0-ms execution time (f_{osc}=8 MHz,1/8 f_{osc}))
Other than * and **
1-byte 1-cycle instruction (1 ROM byte used, 1.0-ms execution time (f_{osc}=8 MHz,1/8 f_{osc}))

CHAPTER 11 PRODUCT WITH ON-CHIP EPROM

11.1 Overview

The MN15P0222 is a product incorporating the components of the MN150222 except for the mask ROM, which is replaced with a 2-Kbyte EPROM (i.e., an electrically programmable ROM), and two additional comparator systems. This EPROM is the same as the on-chip EPROM of the MN150120. For the functions of the comparators, refer to the specifications of the MN150120.

The on-chip EPROM has write and verify specifications conforming to Intel's 27C512. The MN15P0222, however, consists of 20 pins. Therefore, the MN15P0222 cannot fully meet the specifications of the 27C512, which has 28 pins. Therefore, the MN15P0222 incorporates an address generation circuit to address indirectly with an external circuit mounted to a dedicated adapter. In this method, a PROM writer (EPP) as an in-circuit emulator for the PanaX1500 series or a general-purpose PROM writer can be used to write programs to the EPROM. Due to the circuit configuration of the MN15P0222, however, no data can be written to or read from the EPROM with direct addressing. Be aware that not all general-purpose PROM writer models are available for writing data to or reading data from the EPROM.

The MN15P0222-SOP in 20-pin SO package construction and the MN15P0222-SDP in 22-pin SDIL package construction are resin-sealed products. Each of them incorporates an EPROM to which data can be written but the written data cannot be erased.

The PX-AP150222-SOC in 20-pin SO package construction and the PX-AP150222-SDC in 20-pin SDIL package construction are ceramic-sealed products. Each of them incorporates an EPROM to which data can be written and the written data can be erased by applying ultraviolet rays.

11.2 Operation of On-chip EPROM

By setting the CPU of the MN15P0222 to EPROM mode, the MN15P0222 stops functioning as a microcomputer, and the on-chip EPROM is programmable.

Fig 11.2.1 shows the pin assignment in EPROM mode.

(1) Write

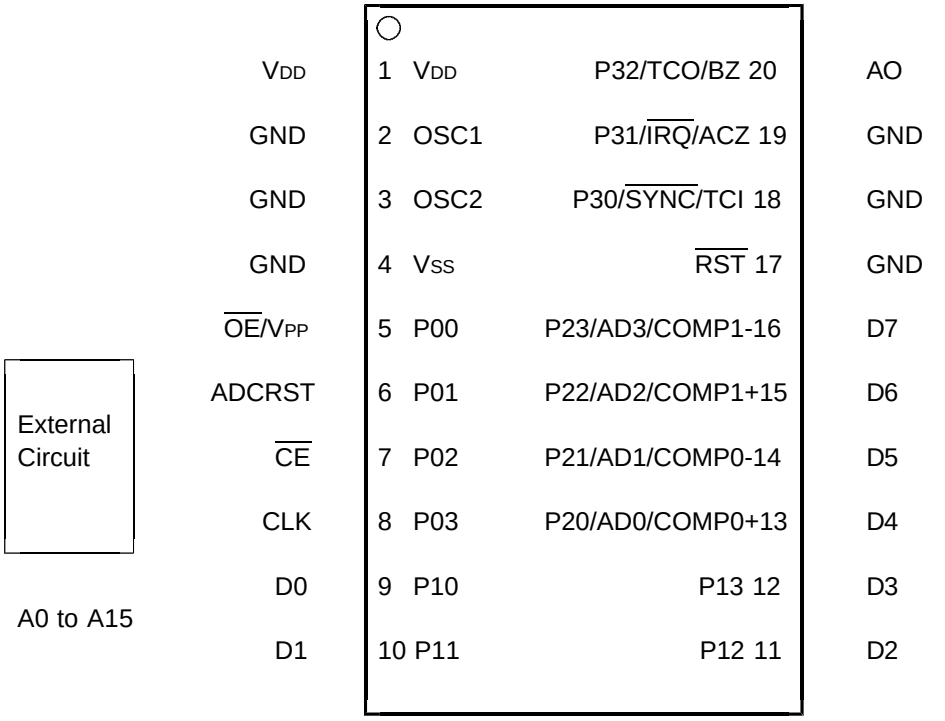
By applying 12.5 V to the $\overline{OE}/V_{PP}$ pin and setting the $\overline{CE}$ pin to low level after setting the supply voltage (V_{DD}) to 6 V, the EPROM is set to program mode. Then the parallel 8-bit data that is input from the data I/O pins D0 to D7 is written to the addresses A0 to A15 generated from the internal address circuit. Refer to Fig. 11.8.1 for the I/O timing in this mode.

(2) Verify

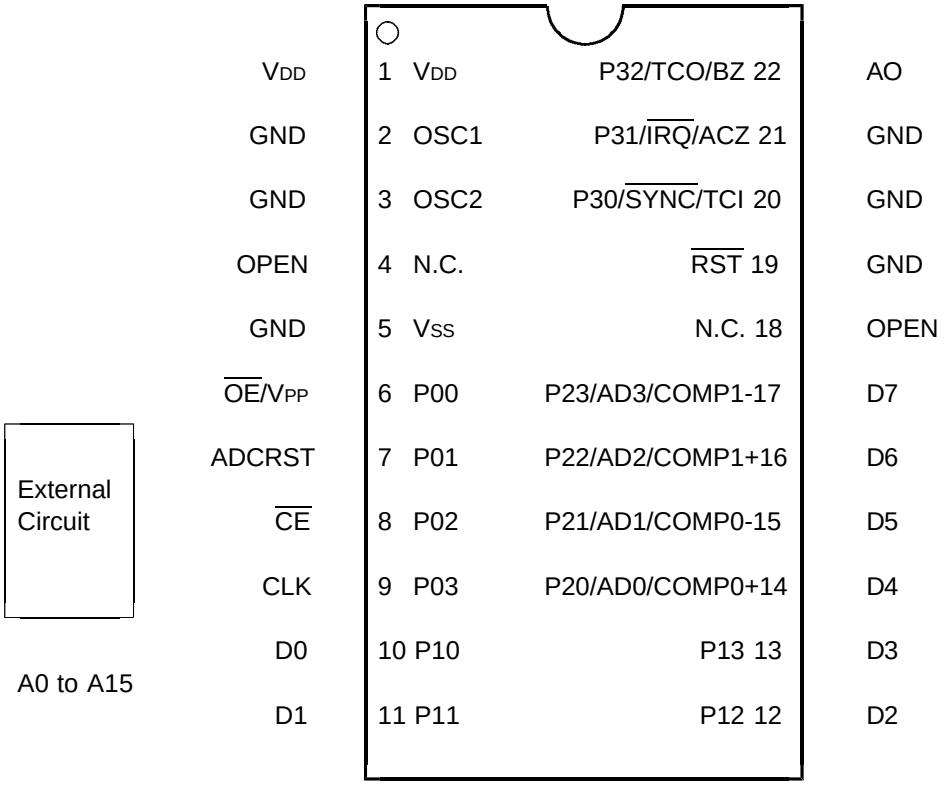
The written data is output from the data I/O pins D0 to D7 by setting both the $\overline{CE}$ pin and $\overline{OE}/V_{PP}$ pin to low level. Then the contents of the data can be verified. Refer to Fig. 11.8.1 for the I/O timing in this mode.

The following table shows the status of each pin according to the mode.

Mode Pin	V_{DD}	$\overline{OE}/V_{PP}$	$\overline{CE}$	D0 to D7	A0 to A15
Write	+6 V	+12.5 V	V_{IL}	Data In	Address In
Verify	+6 V	V_{IL}	V_{IL}	Data Out	Address In
Write/Verify inhibited	+6 V	+12.5 V	V_{IH}	Hi-Z	Don't Care
Read	+5 V	V_{IL}	V_{IL}	Data Out	Address In
Output inhibited	+5 V	V_{IH}	V_{IL}	Hi-Z	Don't Care
Standby	+5 V	Don't Care	V_{IH}	Hi-Z	Don't Care



20-Pin SO Package



22-Pin SDIL Package

Fig. 11.2.1 EPROM Mode Pin Assignment

11.3 EPROM Programmable Option

Mask options can be set in the addresses X 'FFF0' to X 'FFFF' of the on-chip EPROM of the MN15P0222. Table 11.3.1 shows the addresses and corresponding options.

Table 11.3.1 Corresponding Options

Bit / Address	7	6	5	4	3	2	1	0	Classification
FFF0	P13 OFF/ON	P12 OFF/ON	P11 OFF/ON	P10 OFF/ON					Pull-up resistor ON/OFF setting
FFF1	P33 OFF/ON	P32 OFF/ON	P31 OFF/ON	P30 OFF/ON	P23 OFF/ON	P22 OFF/ON	P21 OFF/ON	P20 OFF/ON	
FFF2	P13 PP/N-OD	P12 PP/N-OD	P11 PP/N-OD	P10 PP/N-OD					Pin type selection (See Note 1)
FFF3	P33 PP/N-OD	P32 PP/N-OD	P31 PP/N-OD	P30 PP/N-OD	P23 PP/N-OD	P22 PP/N-OD	P21 PP/N-OD	P20 PP/N-OD	
FFF4			Model selection (See Note 2) MN150222 /MN150120		Watchdog timer OFF/ON	Reset voltage V_{RSTL1}/ V_{RSTL2}	Oscillator frequency High/Low		Others

Selection of options in the above table indicates the setting of each bit to 1 or 0. For example, the P13 pull-up resistor OFF is selected with the bit 7 of address X 'FFF0' set to 1 and the P13 pull-up resistor ON is selected with the bit set to 0.

*1: In the above table, "PP" stands for "push-pull" and "N-OD" stands for "N-ch open-drain."
*2: Make the following settings for model selection.
Both bits 5 and 4 of address X 'FFF4' set to 1: MN150222
Both bits 5 and 4 of address X 'FFF4' set to 0: MN150120

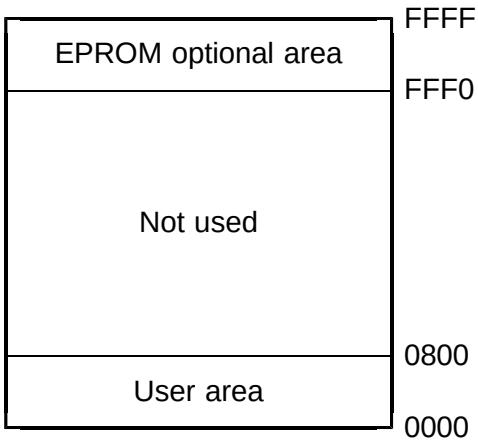
Note 1) Set bits to 1 if the bits are not set to any options.
Note 2) No options are available to the following items.
- Auto reset ON/OFF: Fixed to ON i.e., incorporated. (Select either V_{RSTL1} or V_{RSTL2}.)
- $\overline{RST}$ pin pull-up resistor ON/OFF: Fixed to ON i.e., incorporated.

Note 3) Optional data set condition (Either one of the following conditions.)
- The V_{DD} has exceeded the auto reset clearing voltage V_{RSTH1}.
- The reset status is cleared with high-level input applied to the $\overline{RST}$ pin.

Note 4) While low-level input is applied to the $\overline{RST}$ pin, the oscillator frequency is set to high regardless of the setting in bit 1 of address X 'FFF4'. Therefore, the low-frequency oscillator may abnormally oscillate.

11.4 MN15P0222 Operational Precautions

(1) Unlike the 27C512, data can be written to the 2-Kbyte user area (addresses X '0000' to X '07FF') and the EPROM optional area (addresses X 'FFF0 to X 'FFFF') of the on-chip EPROM of the MN15P0222. Any other address area prohibits data from being written. Therefore, when writing programs, the data in addresses X '0800' to X 'FFEF' must be X 'FF'.



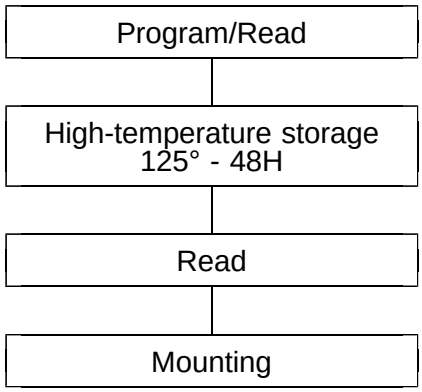
EPROM area

(2) Before writing programs with the PROM writer, be sure to check that the RPOM writer and the CPU are connected properly through a socket adapter. If they are not connected properly, the CPU may be damaged.

(3) Be aware that the MN15P0222 is partly different from the MN150222 and MN150120 in electric characteristics.

(4) After programs are written to the PX-AP15P0222-SOC or PX-AP15P0222-SDC, in order to prevent the data from being lost, put a little baffle seal on the glass portion on the upper side of the package to shut off ultraviolet rays.

(5) It is recommendable to perform high-temperature storage screening after programs are written until the LSI is mounted.



(6) It is not possible to conduct data writing test on all bits of the MN15P0222-SOP or MN15P0222-SDP due to the nature of the device. Therefore, the reliability of the data storage of the device may not be 100% guaranteed.

11.5 Erasing Data from On-chip EPROM

(1) Outline of Function

The PX-AP150222-SOC and PX-AP150222-SDC are of ceramic-sealed package construction incorporating a window each. The data on the on-chip EPROM can be erased by applying 2537-Å ultraviolet rays to the chip through the window so that all the bits of the EPROM will be set to 1.

(2) Procedure

1) Clean the window with alcohol if there is any oil or glue on it. Do not apply organic solvent that may damage the package.
2) Apply the ultraviolet rays for 15 to 20 minutes, provided that the commercial ultraviolet lamp is located 2 to 3 meters above the package. The illumination on the package surface will be 12000îW/m².
   Then there will be an exposure dose of 10 W · S/m² and the data is erased completely.
   - If the lamp has a filter, remove the filter.
   - By attaching a reflector to the lamp, the illumination will be 1.4 to 1.8 times as high.
   - Consequently, the time taken for erasing the data will be shorter.
   - Check the life of the lamp and fully maintain the proper illumination.

(3) Ultraviolet Exposure Dose

The recommendable exposure dose is 10 W·S/m². This is a marginal value. This period is several times as large as an estimated period required to erase the data in each bit. Be sure to keep this value in order to erase the data completely at all the ranges of temperature and supply voltage.

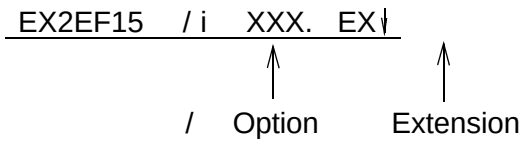
(4) Operational Precautions for Packages Incorporating Window

The data in the EPROM in a package incorporating a window is erased by applying light with a maximum wavelength of 4000 Å.
Although the possibility is very low, the data may be erased by fluorescent light or sunlight. Therefore, exposure to fluorescent light or sunlight for a long time has a bad influence on the reliability of the system.
If the LSI is used under fluorescent light or sunlight, be sure to seal the window so that the chip will be free of such light.
The data in the EPROM is not lost if the wavelength of applied light exceeds a range between 4000 and 5000 Å.
The LSI is, however, a product with general semiconductor characteristics. Therefore, if the LSI is exposed to excessively intensive light, the internal circuit may malfunction.
In the above case, the LSI returns to normal operation with the light shut off. If the LSI is used in places continuously exposed to light with a wavelength exceeding 4000 Å, some countermeasures are required against the light as well.

11.6 Writing Data to On-chip EPROM

(1) Writing PROM Data with Standard PROM Writer
   1) Write the PROM data to the PROM writer.
   2) Mount the MN15P0222 to the PROM writer through a socket adapter.
   3) Write the data in Intel 27C512 mode.
      To operate the PROM writer, refer to the operation manual of the PROM writer.

(2) Writing PC Data with Standard PROM Writer
   1) Connect the PC (personal computer) to the PROM writer through an RS-232C cable.
   2) Open the conversion utility software EX2EF15.EXE and convert the executable file XXX.EX into the Intel HEX format file XXX.HEX with the following command input.



(Note) The Intel HEX file is not generated but only an EF file is generated if no option is input. The extension (.EF) means that the file is in the version 2.0 assembler format or an older assembler format.

(Supplemental Information)
The following setting options are displayed when "EX2EF15" is input.
- /e: Message output in English.
- /h: No help menu output.
- /S: No symbol output to the EF file.
- /W: Executing with less memory capacity.
- /I: Output in Intel HEX format.

   3) Set the PROM writer to Intel 27C512 mode.
   4) Clear all the data in the PROM writer (set to X 'FF').
   5) Set the mode of the PROM writer so that data can be received in the Intel HEX format over RS-232C.
   6) Use the Copy command of the MS-DOS and transfer XXX.HEX from the PC to the PROM writer.
   7) Mount the MN15P0222 to the PROM writer through a socket adapter.
   8) Write the data in Intel 27C512 mode.

Refer to the operation manual of the PROM writer for details.

Table 11.6.1 PROM Writer Evaluation

Manufacturer	Product name	Device type	Result	Conditions
MATSUSHITA ELECTRONICS CORPORATION	EPP	Intel Fast12.5V	OK	Exclusive software (EPP222.EXE) used
Data I/O Corporation	2900	Intel 27C512	OK	Connection test Continuity check = No Electronic signature read Compare electric ID = No
	3900	Intel 27C512	OK	
	LabSite	Intel 27C512	OK	
	PSX500	Intel 27C512	OK	Contact test Device test = No Electronic signature read Electric ID test = No
Minato Electronics Inc.	M1890A/OU910	E610(27512)	OK	
	M1892/TYPE-9132A	E610(27512)	OK	
	M1930/SU3000	E610(27512)	OK	Verify mode (Normal setting)
AVAL DATA Corporation	PKW-1100+RX1	Intel 27C512	NG	
	PKW-3100+ADP. B	Intel 27C512	NG	
	PKW-5100+GX1	Intel 27C512	OK	

11.7 Difference between MN15P0222 and MN150222 or MN150120

Parameter	MN15P0222	MN150222/MN150120	Remarks
ROM	2048 × 8 bits	2048 × 8 bits/1024 × 8 bits	
ROM	96 × 4 bits	96 × 4 bits/64 × 4 bits	
Operating ambient tempertaure	-20 °C to +70 °C	-40 °C to +85 °C	
Operating surpply voltage	Refer to B1 of Chapter 11.8.	Refer to B1 of Chapter 1.7.	See Note 1)
Operating supply current	Refer to C1 to C4 of Chapter 11.8.	Refer to C1 to C4 of Chapter 1.7.	See Note 2)
P00	Refer to A5 and C7 of Chapter 11.8.	Refer to A5 and C7 of Chapter 1.7.	Shared with V_{PP} pin.
Auto reset voltage level	Refer to B5 of Chapter 11.8.	Refer to B5 of Chapter 1.7.	
A/D conversion relative accuracy	±6	±3	
Option	EPROM option (Refer to Chapter 11.4.)	Mask option (Refer to check list.)	

- For latch-up prevention, insert a bypass capacitor that has a minimum capacitance of 680 pF between the MN15P0222's power supply and ground pins.
- Evaluate the oscillation and EMC (electro-magnetic compatibility) noise characteristics of each model individually because they may change according to the mask pattern layout.

Note 1) The minimum guaranteed operating voltage of the MN15P0222 is 2.35 V.
Note 2) The current consumption of the MN15P0222 is a little higher than that of the MN150222 or MN150120.

11.8 Electrical Characteristics (See Note 1.)

Type	MOS LSI
Function	CMOS 4-bit single-chip microcomputer

A. Absolute Maximum Ratings Ta = 25 °C, V_{SS} = 0V

	Parameter	Symbol	Rating	Unit
A1	Supply voltage (See Note 2)	V_{DD}	-0.3 to +7.0	V
A2	Input clamp current (P31/IRQ/ACZ)	I_C	-0.5 to +0.5	mA
A3	Input pin voltage	V_I	-0.3 to V_{DD} +0.3 * Not applicable to P31/IRQ/ACZ	V
A4	Output pin voltage	V_O	-0.3 to V_{DD} +0.3	V
A5	High-current output pin voltage	V_{OH}	-0.3 to +7.0 * Not applicable to P00	V
A6	I/O pin voltage	V_{IO}	-0.3 to V_{DD} +0.3	V
A7	Peak output current (Other than P0)	$I_{OH(Peak)}$ $I_{OL(Peak)}$	-10 20	mA
A8	Peak output current (P0)	$I_{OL(Peak)}$	40	mA
A9	Average output current (See Note 3.) (Other than P0)	$I_{OH(avg)}$ $I_{OL(avg)}$	-2 10	mA
A10	Average output current (See Note 3.) (P0)	$I_{OL(avg)}$	15	mA
A11	Power dissipation	P_D	See Note 4.	mW
A12	Operating ambient temperature	T_{opr}	-20 to +70	°C
A13	Storage temperature	T_{stg}	-55 to +125	°C

Note 1) Those electrical characteristics are reference values. For details, refer to the Product Standards.

Note 2) To prevent latch-up, connect one or more 680 pF or larger bypass capacitors between the power supply pins and ground.

Note 3) Applied to any 100ms period.
Make sure that the total output current value of all output pins is 30 mA or less for 20-pin SOP and 50 mA or less for 22-pin SDIP.

Note 4) 22-pin SDIP: P_D = 350 mW
20-pin SOP : P_D = 180 mW

B. Operating Conditions

Ta = -20 °C to +70 °C, V_{DD} = 2.35 V to 5.5 V (V_{RSTL1} to 5.5 V), V_{SS} = 0 V

See Note.

Parameter		Symbol	Conditions	Limits			Unit
				min	typ	max	
B1	Supply voltage	V_{DD1}	Machine cycle: 1.0 ms High-speed oscillation mode	4.5	5.0	5.5	V
		V_{DD2}	Machine cycle: 4.0 ms High-speed oscillation mode with auto reset (Standard V_{DD} = 3 V)	2.35 See Note 2)		5.5	
		V_{DD3}	Machine cycle: 4.0 ms High-speed oscillation mode with auto reset (Standard V_{DD} = 5V)	V_{RSTL1}		5.5	
		V_{DD4}	Machine cycle: 64.0 ms Low-speed oscillation mode with auto reset (Standard V_{DD} = 3V)	2.35 See Note 2)		5.5	
		V_{DD5}	Machine cycle: 64.0 ms Low-speed oscillation mode with auto reset (Standard V_{DD} = 5 V)	V_{RSTL1}		5.5	

Note 1) The V_{RSTL1} voltage refers to the supply voltage that is detected to reset the LSI, which is applied if the auto reset voltage is set to a standard V_{DD} of 5 V as an EPROM option.

Note 2) The product incorporates an auto reset function that is always available. If the operation voltage is comparatively low, set the auto reset voltage to a standard V_{DD} of 3 V as an EPROM option. In that case, however, the auto reset function may be activated regardless of the minimum guaranteed voltage of V_{DD} (i.e., 2.35 V) and the microcomputer may be reset.

Auto Reset Circuit 1

B2	Voltage detection level	V_{RSTH1}	Fig. 1		3.1	4.0	V
		V_{RSTL1}		2.0	3.0		
B3	Hysteresis width	V_H		0.05	0.1		
B4	Supply voltage change rate	D t/D V		1.00			ms/V

* The above values are applied if the auto reset voltage is set to a standard V_{DD} of 5 V as an EPROM option.

Auto Reset Circuit 2

B5	Voltage detection level	V_{RSTH2}	Fig. 1		2.4	2.6	V
		V_{RSTL2}		1.5	2.2		
B6	Hysteresis width	V_H		0.05	0.1		
B7	Supply voltage change rate	D t/D V		1.00			ms/V

* The above values are applied if the auto reset voltage is set to a standard V_{DD} of 3 V as an EPROM option.

Note) The guaranteed operating V_{DD} range of the product is between 2.35 V and 5.50 V. Therefore, the microcomputer may be out of control before the reset function is activated in the above case.

Operating Speed

Ta = -20 °C to +70 °C, V_{DD} = 2.35 V to 5.5 V (V_{RSTL1} to 5.5 V), V_{SS} = 0 V

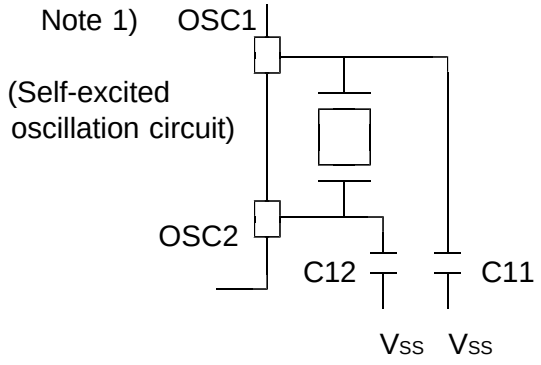
Parameter		Symbol	Conditions	Limits			Unit
				min	typ	max	
B8	Instruction execution time	t_{c1}	V_{DD} = 4.5 V to 5.5 V High-speed oscillation mode f_{osc} = 8.0 MHz		1.0		ms
		t_{c2}	V_{DD} = 2.35 V to 5.5 V High-speed oscillation mode f_{osc} = 2.0MHz Auto reset: ON (Standard V_{DD} = 3 V)		4.0		
		t_{c3}	V_{DD} = V_{RSTL1} to 5.5 V High-speed oscillation mode f_{osc} = 2.0 MHz Auto reset: ON (Standard V_{DD} = 5 V)		4.0		
		t_{c4}	V_{DD} = 2.35 V to 5.5 V Low-speed oscillation mode f_{osc} = 125 kHz Auto reset: ON (Standard V_{DD} = 3 V)		64.0		
		t_{c5}	V_{DD} = V_{RSTL1} to 5.5 V Low-speed oscillation mode f_{osc} = 125 kHz Auto reset: ON (Standard V_{DD} = 5 V)		64.0		

Oscillation OSC1, OSC2 (See Note 1.) (Select the oscillation mode as an EPROM option.)

B9	Oscillator frequency	f_{Xtal1}	V_{DD} = 2.35 V to 5.5 V High-speed oscillation mode	0.5		8.0	MHz
		f_{Xtal2}	V_{DD} = 2.35 V to 5.5 V Low-speed oscillation mode	32		125	kHz

* Regardless of EPROM optional settings in the product, the product is fixed at high-frequency oscillation mode in the external RST status (i.e., the RST pin is at low level), when there may be no oscillation.

Note 1)



- Have the sample of the above circuits evaluated by oscillator manufacturer to determine the external capacitance each of C11 and C12. In most cases, the appropriate value of each capacitor seems to be approx. 30 pF.
- The LSI has an on-chip feedback resistor.

External Clock Input 1 OSC1 (High-speed oscillation mode as an EPROM option. OSC2 is open.)
Ta = -20 °C to +70 °C, V_{DD} = 2.35 V to 5.5 V (V_{RSTL1} to 5.5 V), V_{SS} = 0 V

Parameter		Symbol	Conditions	Limits			Unit
				min	typ	max	
B10	Clock frequency	f_{osc1}		1.0		8.0	MHz
	High-level pulse width *	t_{wh1}	Fig. 2 A clock duty ratio should be 45 % to 55 %.	40			ns
	Low-level pulse width *	t_{wl1}		40			
	Rise time	t_{wr1}	Fig. 2			20	
	Fall time	t_{wf1}				20	
	Input voltage high level	V_{IH1}		0.8V_{DD}		V_{DD}	V
	Input voltage low level	V_{IL1}		V_{SS}		0.2V_{DD}	

External Clock Input 2 OSC1 (Low-speed oscillation mode as an EPROM option. OSC2 is open.)

B11	Clock frequency	f_{osc1}		32		125	MHz
	High-level pulse width *	t_{wh1}	Fig. 2 A clock duty ratio should be 45% to 55%.	0.8			ns
	Low-level pulse width *	t_{wl1}		0.8			
	Rise time	t_{wr1}	Fig. 2			20	
	Fall time	t_{wf1}				20	
	Input voltage high level	V_{IH1}		0.8V_{DD}		V_{DD}	V
	Input voltage low level	V_{IL1}		V_{SS}		0.2V_{DD}	

External Clock Input 3 TCI

Ta = -20 °C to +70 °C, V_{DD} = 2.35 V to 5.5 V (V_{RSTL1} to 5.5 V), V_{SS} = 0 V

Parameter		Symbol	Conditions	Limits			Unit
				min	typ	max	
B12	Clock frequency	f_{tci}	V_{DD} = 2.35 V to 5.5 V Fig. 3			5	MHz
	High-level pulse width *	t_{wh2}		100			ns
	Low-level pulse width *	t_{wl2}		100			
	Rise time	t_{rcp}	Fig. 3			20	
	Fall time	t_{fcp}				20	
	Input voltage high level	V_{IH2}		0.8V_{DD}		V_{DD}	V
	Input voltage low level	V_{IL2}		V_{SS}		0.1V_{DD}	

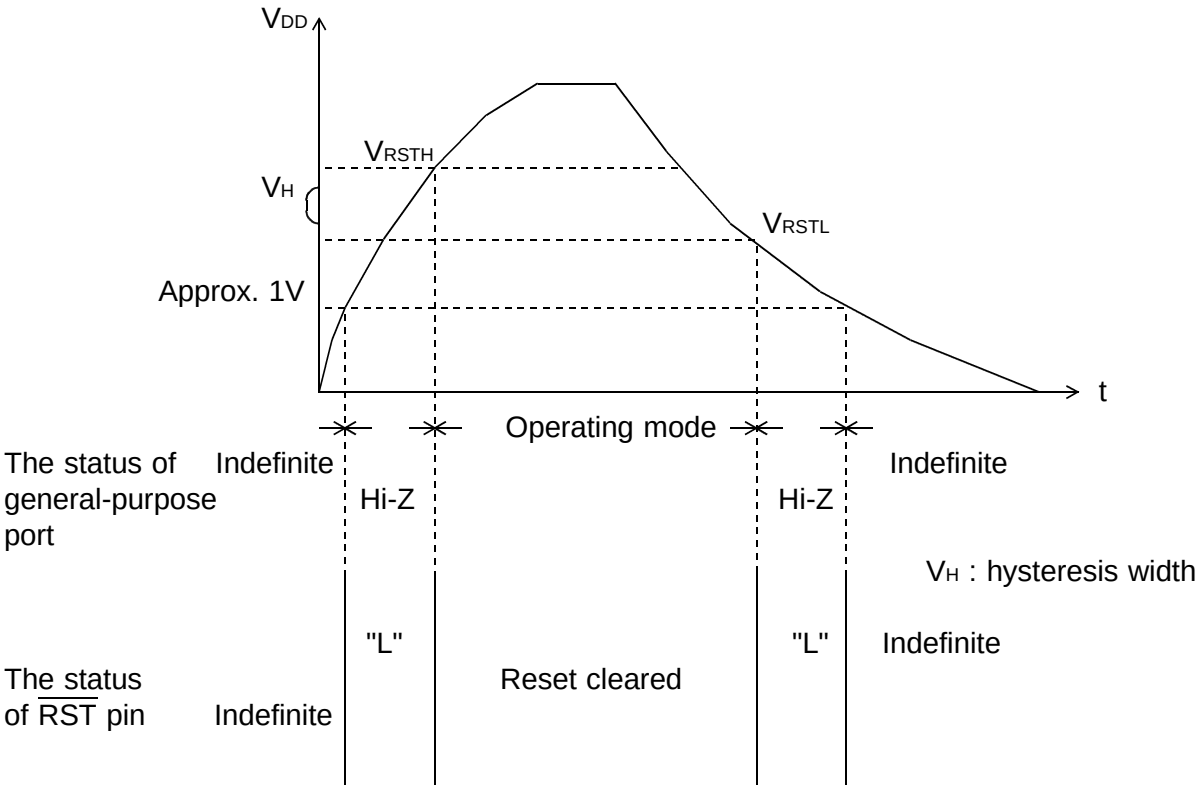


Fig. 1 Auto Reset Voltage

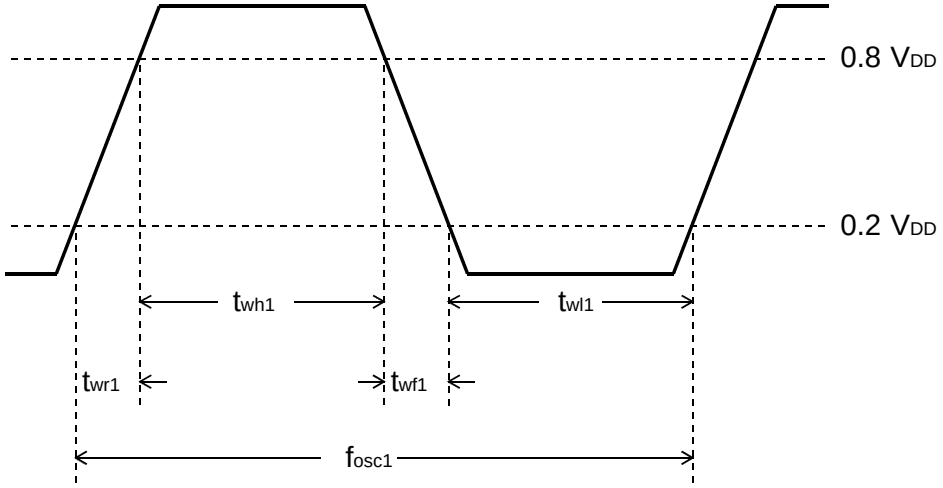


Fig. 2 OSC1 Timing Chart

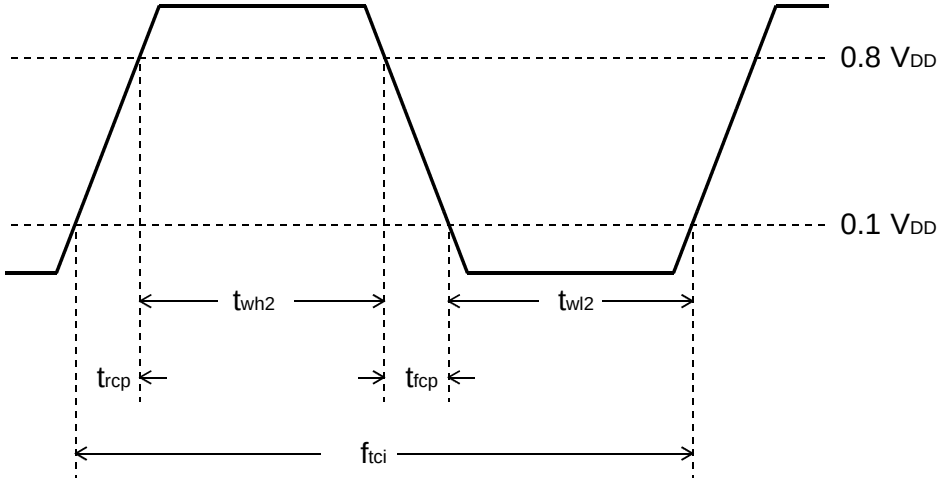


Fig. 3 TCI Timing Chart

C. Electrical Characteristics (DC Characteristics)

Ta = -20 °C to +70 °C, V_{DD} = 2.35 V to 5.5 V (V_{RSTL1} to 5.5 V), V_{SS} = 0 V

Parameter	Symbol	Conditions	Limits			Unit
			min	typ	max	
Supply Current						
C1 Operating supply current	I_{DD1}	f_{osc} = 8.0 MHz V_{DD} = 5.0 V		4.0	8.0	mA
	I_{DD2}	f_{osc} = 32.768 kHz V_{DD} = 5.0 V		0.7	2.0	
C2 Supply current in HALT mode	I_{DD3}	f_{osc} = 32.768 kHz V_{DD} = 5.0 V		15.0	30.0	mA
C3 Supply current in STOP mode	I_{DD4}	V_{DD} = 5.0 V		0.5	5.0	
C4 Auto reset current consumption	I_{DD5}	V_{DD} = 5.0 V, 3.0 V		8.0	80.0	

- Make measurement at Ta = 25 °C while under no-load condition.
- The operating supply current, I_{DD1}, applies if the high-speed oscillation mode is selected as an EPROM option. To measure this current, fix the I/O pins to V_{DD} level in the RESET mode, and input an 8-MHz square-wave, which swings between V_{DD} and V_{SS} voltage levels, into the OSC1 pin.
- The operating supply current, I_{DD2}, applies if the low-speed oscillation mode is selected as an EPROM option. To measure this current, clear the RESET mode, fix the I/O pins to V_{DD} level during execution of NOP instruction, and input a 32.768-kHz square wave, which swings between V_{DD} and V_{SS} voltage levels, into the OSC1 pin.
- The supply current in HALT mode, I_{DD3}, applies if the low-speed oscillation mode is selected as an EPROM option. To measure this current, clear the RESET mode, and set to the HALT mode, and, after fixing the I/O pins to V_{DD} level, input a 32.768-kHz square wave, which swings between V_{DD} and V_{SS} voltage levels, into the OSC1 pin.
- To measure the supply current in STOP mode, I_{DD4}, clear the RESET mode and set to the STOP mode. Then fix the I/O pins to V_{DD} level and open OSC1 pin.
- Auto reset current consumption, I_{DD5}, refers to the constant current consumption of the auto reset circuit. Therefore, the value of current consumption is added to each supply current rating.

Ta = -20 °C to +70 °C, V_{DD} = 2.35 V to 5.5 V (V_{RSTL1} to 5.5 V), V_{SS} = 0 V

	Parameter	Symbol	Conditions	Limits			Unit
				min	typ	max	
	High-Current I/O Pin P00 (N-ch open-drain)						
C5	Input voltage high level	V_{IH1}		0.7V_{DD}		V_{DD}	V
C6	Input voltage low level	V_{IL1}		V_{SS}		0.3V_{DD}	
C7	Output leakage current	O_{LK1}	Output: Hi-Z V_{IN} = 0 V to V_{DD}			±10	mA
C8	Output voltage low level	V_{OL1}	I_{OL} = 20.0 mA V_{DD} = 5.0 V	V_{SS}		2.0	V
	High-Current I/O Pins P01 to P03 (N-ch open-drain)						
C9	Input voltage high level	V_{IH1}		0.7V_{DD}		V_{DD}	V
C10	Input voltage low level	V_{IL1}		V_{SS}		0.3V_{DD}	
C11	Output leakage current	O_{LK1}	Output: Hi-Z V_{IN} = 0 V to 6 V			±10	mA
C12	Output voltage low level	V_{OL1}	I_{OL} = 20.0 mA V_{DD} = 5.0 V	V_{SS}		2.0	V
	I/O Pins P10 to P13 P20/AD0/COMP0+ to P23/AD3/COMP1- (When the pins are used as P20 to P23 pins) P30/$\overline{SYNC}$/TCI, P31/$\overline{IRQ}$/ACZ, P32/TCO/BZ (When the pins are used as P30/$\overline{SYNC}$, P31, P32/TCO/BZ pins)						
C13	Input voltage high level	V_{IH2}		0.7V_{DD}		V_{DD}	V
C14	Input voltage low level	V_{IL2}		V_{SS}		0.3V_{DD}	
C15	Input current	I_{I2}	With pull-up resistor V_{IN} = 1.5 V V_{DD} = 5.0 V	-50	-120	-300	mA
C16	Input leakage current	I_{LK2}	Without pull-up resistor V_{IN} = 0 V to V_{DD}			±1	
C17	Output voltage high level	V_{OH2}	I_{OH} = -500 mA V_{DD} = 5.0 V	4.5		V_{DD}	V
C18	Output voltage low level	V_{OL2}	I_{OL} = 3.5 mA V_{DD} = 5.0 V	V_{SS}		0.5	

Note) Use the P30/$\overline{SYNC}$/TCI pin under the following condition:
The load must be set so that the output voltage high level will be more than 0.8 V_{DD} while the $\overline{SYNC}$ timing signal is output. That is, at the time the LSI is reset or within two machine cycles after the reset status of the LSI is cleared.

* Setting of each pin is possible as an EPROM option.

Ta = -20 °C to +70 °C, V_{DD} = 2.35 V to 5.5 V (V_{RSTL1} to 5.5 V), V_{SS} = 0 V

	Parameter	Sym-bol	Conditions	Limits			Unit
				min	typ	max	

Input Pins P20/AD0 to P23/AD3 (When the pins are used as A/D input pins)

C19	Converted voltage range	V_{AD}		V_{SS}		V_{DD}	V
C20	Resolution					10	bit
C21	Relative precision		V_{DD} = 5.0 V V_{SS} = 0.0 V			±6	LSB
C22	Zero transition voltage	V_{0T}			20	60	mV
C23	Full-scale transition voltage	V_{FST}			V_{DD} -20	V_{DD} -60	
C24	A/D conversion time		f_{osc} = 8 MHz V_{DD} = 5.0 V V_{SS} = 0.0 V		15.00	27.00 See Note.	ms
C25	Sampling time		f_{osc} = 8 MHz V_{DD} = 5.0 V V_{SS} = 0.0 V		4.00	16.00 See Note.	ms
C26	Analog input voltage	V_{ADIN}		V_{SS}		V_{DD}	V
C27	Analog input leakage current		V_{ADIN} = 0 V to V_{DD} (V_{ADIN} when channel is off.)		±.001	±1	mA
C28	Ladder resistance	R_{ladd}		10	50	100	kW

Note) The value is applied when bp3 (ADTC) of the A/D control register ADCL is set to zero.

Relative precision:

The deviation of the converted straight line from the ideal straight line that results after both the zero transition voltage and full-scale transition voltage are adjusted to zero.

Zero transition voltage:

Indicates the difference between the analog input voltage and the nominal value when the digital output code changes from 0 (000h) to 1 (001h).

Full-scale transition voltage:

Indicates the difference between the analog input voltage and the nominal value when the digital output code (3FEh) reaches the full-scale value (3FFh).

* Be sure to select a necessary EPROM option so that no pull-up resistor will be connected to any pins working as A/D input pins.

Ta = -20 °C to +70 °C, V_{DD} = 2.35 V to 5.5 V (V_{RSTL1} to 5.5 V), V_{SS} = 0 V

Parameter	Sym-bol	Conditions	Limits			Unit
			min	typ	max	

Input Pin P31/$\overline{IRQ}$/ACZ (When this pin is used as ACZ pin)

C29	ACZ input (high-level output)	V_{SH}	Fig. 5	1.5		V_{DD} -1.5	V
C30	ACZ input (low-level output)	V_{SL}	V_{DD} = 4.5 V to 5.5 V	V_{SS}		0.5	
				V_{DD} -0.5		V_{DD}	
C31	Input leakage current	I_{LK3}	Without pull-up resistor V_{IN} = 0 V to V_{DD}			±1	mA
C32	Input clamp current	I_{C3}	$V_{IN} > V_{DD}$ $V_{IN} < V_{SS}$ V_{DD} = 5.0 V			±400	

* Be sure to select a necessary EPROM option so that no pull-up resistor will be connected to any pins working as ACZ pins.

I/O Pin P31/$\overline{IRQ}$/ACZ (Schmitt input when this pin is used as $\overline{IRQ}$ pin)

C33	Input voltage highlevel	V_{IH4}		0.8V_{DD}		V_{DD}	V
C34	Input voltage low level	V_{IL4}		V_{SS}		0.1V_{DD}	
C35	Input current	I_{I4}	With pull-up resistor V_{IN} = 1.5 V V_{DD} = 5.0 V	-50	-120	-300	mA
C36	Input leakage current	I_{LK4}	Without pull-up resistor V_{IN} = 0 V to V_{DD}			±1	

* Pull-up resistor is set to ON or OFF by selecting a necessary EPROM option.

I/O Pin P30/$\overline{SYNC}$/TCI (Schmitt input when this pin is used as TCI pin)

C37	Input voltage high level	V_{IH5}		0.8V_{DD}		V_{DD}	V
C38	Input voltage low level	V_{IL5}		V_{SS}		0.1V_{DD}	
C39	Input current	I_{I5}	With pull-up resistor V_{IN} =1.5V V_{DD} =5.0V	-50	-120	-300	mA
C40	Input leakage current	I_{LK5}	Without pull-up resistor V_{IN} = 0 V to V_{DD}			±1	

* Pull-up resistor is set to ON or OFF by selecting a necessary EPROM option.

Ta = -20 °C to +70 °C, V_{DD} = 2.35 V to 5.5 V (V_{RSTL1} to 5.5 V), V_{SS} = 0 V

Parameter		Symbol	Conditions	Limits			Unit
				min	typ	max	
I/O Pin $\overline{RST}$ (Schmitt input)							
C41	Input voltage high level	V_{IH6}		0.8V_{DD}		V_{DD}	V
C42	Input voltage low level	V_{IL6}		V_{SS}		0.1V_{DD}	
C43	Input current	I_{I6}	With pull-up resistor V_{IN} = 1.5 V V_{DD} = 5.0 V	-50	-120	-300	mA
C44	Output voltage low level	V_{OL6}	V_{DD} = 2 V, I_{OL} = 0.3 mA	V_{SS}		0.4	V
Input Pins P20/COMP0 + to P23/COMP1 - (When those pins are used as comparator input pins)							
C45	Input offset voltage	V_{IOF7}	V_{IN} =1.5V to 3.5V		20	100	V
C46	Common-mode input voltage range		V_{DD} = 5.0 V	1.5		3.5	
C47	Input leakage current	I_{LK7}	Without pull-up resistor V_{IN} = 0 V to V_{DD}			±1	mA

* If the comparator function is used, select necessary EPROM options so that the MN150120 will be selected and no pull-up resistor will be connected to any pins working as comparator input pins.

D. Electrical Characteristics (AC Characteristics)

Ta = -20 °C to +70 °C, V_{DD} = 2.35 V to 5.5 V (V_{RSTL1} to 5.5 V), V_{SS} = 0 V

Parameter	Symbol	Conditions	Limits			Unit
			min	typ	max	

$\overline{RST}$ Pin

D1	Effective pulse width	t_{wRST}	Fig. 4	1			mc

* The above pin may not be reset if the pulse width is shorter than the effective pulse width.

(mc: Machine cycle)

P31/$\overline{IRQ}$/ACZ (When this pin is used as ACZ pin)

D2	Rise time	t_{rs}	Fig. 5	30			ms
D3	Fall time	t_{fs}		30			

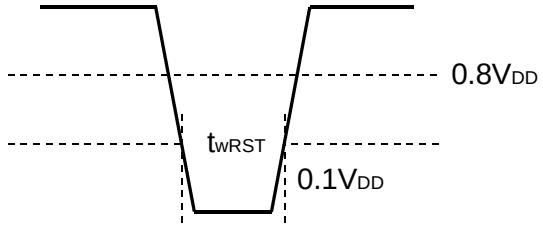


Fig. 4 RST Input Pulse Width

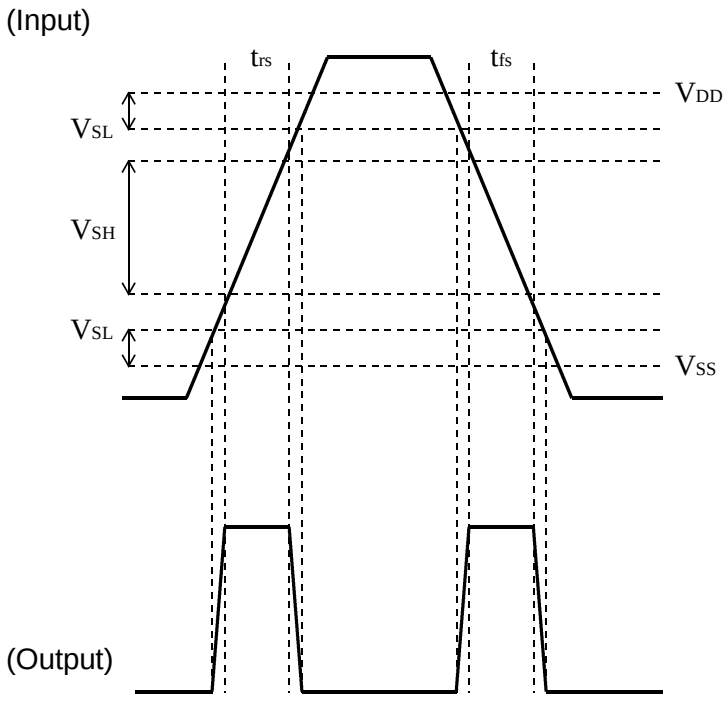


Fig. 5 AC Zero Voltage Detection Circuit Operating Diagram

E. On-chip EPROM Programming Electrical Characteristics

DC Characteristics (V_{DD} = 6 V±0.25 V, V_{PP} = 12.5 V±0.3 V, Ta = 25 °C±5 °C)

	Parameter	Symbol	Conditions	Limits			Unit
				min	typ	max	
Supply Current							
E1	Supply current 1	I_{DD}				30	mA
E2	Supply current 2	I_{PP}				15	
Input Pins	A0 to A15, $\overline{CE}$, $\overline{OE}$ (With 12.5-V voltage not applied to the pins)						
E3	Input voltage high level	V_{IH}	V_{DD} = 6.0 V	2.40		V_{DD}	V
E4	Input voltage low level	V_{IL}	V_{DD} = 6.0 V	V_{SS}		0.45	
E5	Input leakage current	I_L	V_{IN} = 0 V to V_{DD}			±1	mA
I/O Pins	D0 to D7						
E6	Output voltage high level	V_{OH}	V_{DD} = 5.0 V I_{OH} = -500 mA	4.50		V_{DD}	V
E7	Output voltage low level	V_{OL}	V_{DD} = 5.0 V I_{OL} = 3.5 mA	V_{SS}		0.50	
E8	Input voltage high level	V_{IH}	V_{DD} = 6.0 V	2.40		V_{DD}	V
E9	Input voltage low level	V_{IL}	V_{DD} = 6.0 V	V_{SS}		0.45	
E10	Input leakage current	I_L	V_{IN} = 0 V to V_{DD}			±1	ì1A

1. Apply the V_{PP} power supply at 12.5 V after the V_{DD} power supply is fixed at 6.0 V. Turn off the V_{PP} power supply before turning off the V_{DD} power supply.
2. Make sure that the V_{PP} voltage does not exceed 13.5 V including overshooting.
3. Do not dismount or mount the device with 12.5 V applied to the V_{PP} pin, otherwise the reliability of the device may be adversely affected.
4. Do not change the V_{PP} voltage from 12.5 V to the V_{IL} voltage or vice versa while the $\overline{CE}$ pin is at V_{IL} voltage.

AC Characteristics (V_{DD} = 6V±0.25 V, V_{PP} = 12.5 V±0.3 V, Ta = 25 °C±5 °C)

Parameter		Symbol	Conditions	Limits			Unit
				min	typ	max	
E11	Address setup time	t_{AS}		2			ms
E12	$\overline{OE}/V_{PP}$ setup time	t_{OES}		2			ms
E13	Data setup time	t_{DS}		2			ms
E14	Address hold time	t_{AH}		0			ms
E15	Data hold time	t_{DH}		2			ms
E16	V_{DD} setup time	t_{VCS}		2			ms
E17	V_{PP} setup time	t_{VPS}		2			ms
E18	Program pulse width	t_{PW}		0.95	1.0	1.05	ms
E19	Additional program pulse width	t_{OPW}		2.85		78.75	ms
E20	$\overline{CE}$ setup time	t_{CES}		2			ms
E21	$\overline{OE}/V_{PP}$ output delay time	t_{OE}		0		150	ms

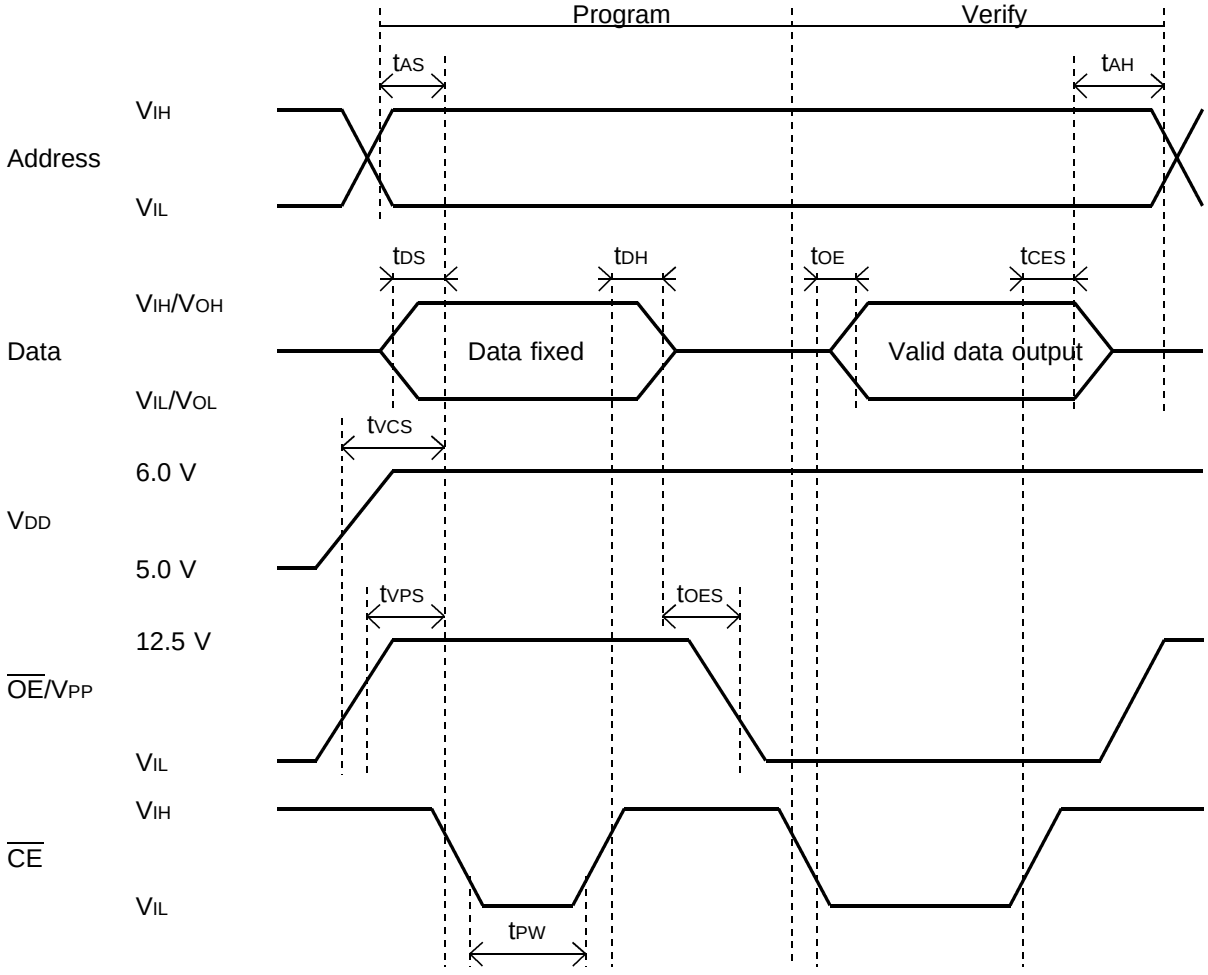


Fig. 11.8.1 I/O Timing during Programming

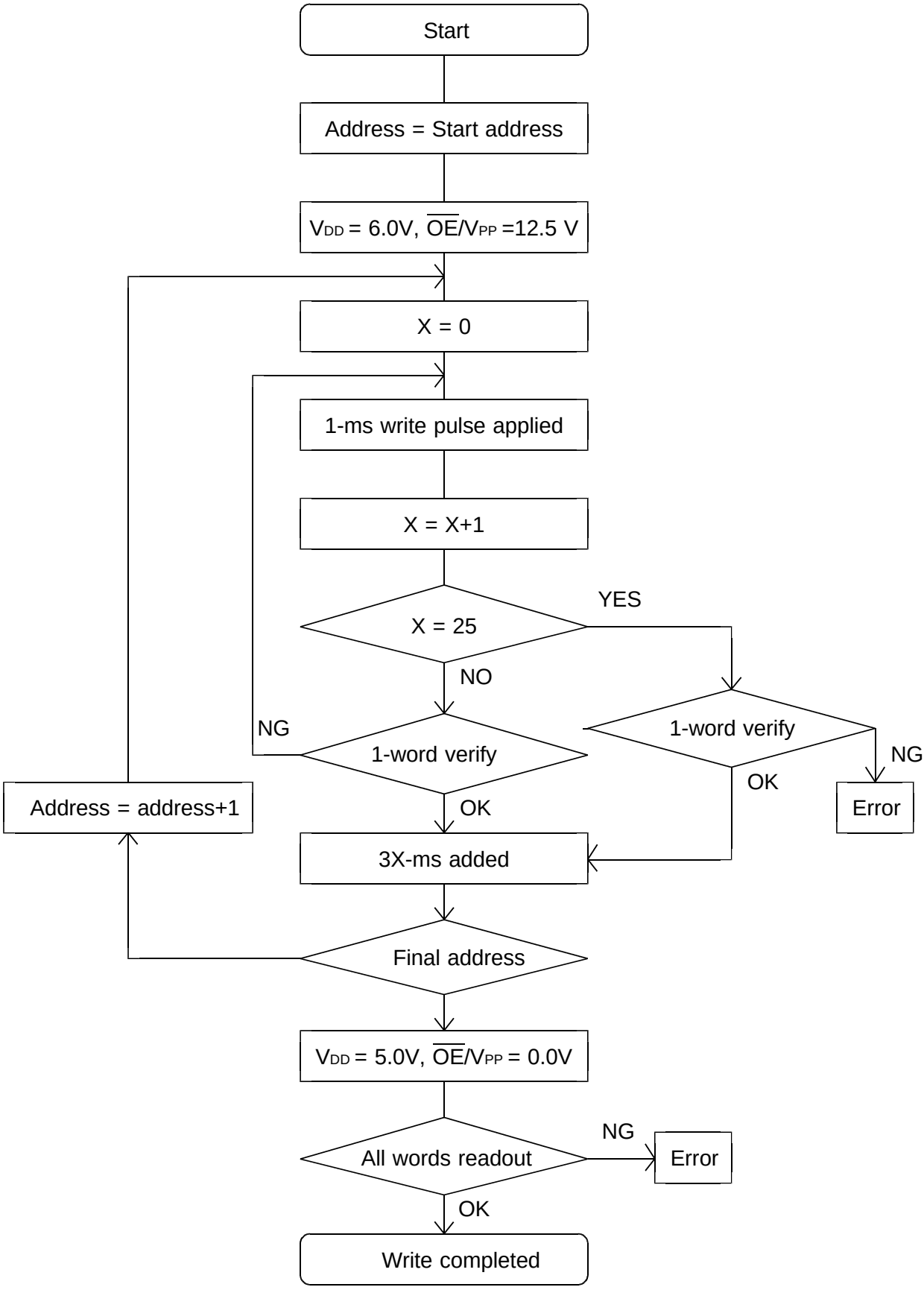


Fig. 11.8.2 Program flow chart

MN150222/P0222

LSI User's Manual

December, 2000 3rd Edition

Issued by Matsushita Electric Industrial Co.,Ltd.

Matsushita Electronics Corporation

© Matsushita Electric Industrial Co., Ltd.
© Matsushita Electronics Corporation

Semiconductor Company, Matsushita Electronics Corporation

Nagaokakyo, Kyoto, 617-8520 Japan
Tel: (075) 951-8151
http://www.mec.panasonic.co.jp

SALES OFFICES

■ U.S.A. SALES OFFICE

Panasonic Industrial Company [PIC]

- **New Jersey Office:**
  2 Panasonic Way, Secaucus, New Jersey 07094
  Tel: 201-392-6173
  Fax: 201-392-4652
- **Milpitas Office:**
  1600 McCandless Drive, Milpitas, California 95035
  Tel: 408-945-5630
  Fax: 408-946-9063
- **Chicago Office:**
  1707 N. Randall Road, Elgin, Illinois 60123-7847
  Tel: 847-468-5829
  Fax: 847-468-5725
- **Atlanta Office:**
  1225 Northbrook Parkway, Suite 1-151,
  Suwanee, Georgia 30174
  Tel: 770-338-6940
  Fax: 770-338-6849
- **San Diego Office:**
  9444 Balboa Avenue, Suite 185
  San Diego, California 92123
  Tel: 619-503-2940
  Fax: 619-715-5545

■ CANADA SALES OFFICE

Panasonic Canada Inc. [PCI]
5700 Ambler Drive Mississauga, Ontario, L4W 2T3
Tel: 905-624-5010
Fax: 905-624-9880

■ GERMANY SALES OFFICE

Panasonic Industrial Europe G.m.b.H. [PIEG]

- **Munich Office:**
  Hans-Pinsel-Strasse 2 85540 Haar
  Tel: 89-46159-156
  Fax: 89-46159-195

■ U.K. SALES OFFICE

Panasonic Industrial Europe Ltd. [PIEL]

- **Electric component Group:**
  Willoughby Road, Bracknell, Berkshire RG12 8FP
  Tel: 1344-85-3773
  Fax: 1344-85-3853

■ FRANCE SALES OFFICE

Panasonic Industrial Europe G.m.b.H. [PIEG]

- **Paris Office:**
  270, Avenue de President Wilson
  93218 La Plaine Saint-Denis Cedex
  Tel: 14946-4413
  Fax: 14946-0007

■ ITALY SALES OFFICE

Panasonic Industrial Europe G.m.b.H. [PIEG]

- **Milano Office:**
  Via Lucini N19, 20125 Milano
  Tel: 2678-8266
  Fax: 2668-8207

■ TAIWAN SALES OFFICE

Panasonic Industrial Sales Taiwan Co.,Ltd. [PIST]

- **Head Office:**
  6th Floor, Tai Ping & First Building No.550. Sec.4,
  Chung Hsiao E. Rd. Taipei 10516
  Tel: 2-2757-1900
  Fax: 2-2757-1906
- **Kaohsiung Office:**
  6th Floor, Hsien 1st Road Kaohsiung
  Tel: 7-223-5815
  Fax: 7-224-8362

■ HONG KONG SALES OFFICE

Panasonic Shun Hing Industrial Sales (Hong Kong) Co., Ltd. [PSI(HK)]
11/F, Great Eagle Centre, 23 Harbour Road,
Wanchai, Hong Kong.
Tel: 2529-7322
Fax: 2865-3697

■ SINGAPORE SALES OFFICE

Panasonic Semiconductor of South Asia [PSSA]
300 Beach Road # 16-01
The Concourse Singapore 199555
Tel: 390-3688
Fax: 390-3689

■ MALAYSIA SALES OFFICE

Panasonic Industrial Company (Malaysia) Sdn. Bhd.

- **Head Office: [PICM]**
  Tingkat 16B Menara PKNS PJ No.17,Jalan Yong
  Shook Lin 46050 Petaling Jaya Selangor Darul Ehsan
  Malaysia
  Tel: 03-7516606
  Fax: 03-7516666
- **Penang Office:**
  Suite 20-17,MWE PLAZA No.8,Lebuh Farquhar,10200
  Penang Malaysia
  Tel: 04-2625550
  Fax: 04-2619989
- **Johore Sales Office:**
  39-01 Jaran Sri Perkasa 2/1,Taman Tampoi
  Utama,Tampoi 81200 Johor Bahru,Johor Malaysia
  Tel: 07-241-3822
  Fax: 07-241-3996

■ CHINA SALES OFFICE

Panasonic SH Industrial Sales (Shenzhen) Co., Ltd. [PSI(SZ)]
7A-107, International Business & Exhibition Centre,
Futian Free Trade Zone, Shenzhen 518048
Tel: 755-359-8500
Fax: 755-359-8516

Panasonic Industrial (Shanghai) Co., Ltd. [PICS]
1F, Block A, Development Mansion, 51 Ri Jing Street,
Wai Gao Qiao Free Trade Zone, Shanghai 200137
Tel: 21-5866-6114
Fax: 21-5866-8000

■ THAILAND SALES OFFICE

Panasonic Industrial (Thailand) Ltd. [PICT]
252/133 Muang Thai-Phatra Complex Building,31st
Fl.Rachadaphisek Rd.,Huaykwang,Bangkok 10320
Tel: 02-6933407
Fax: 02-6933423

■ KOREA SALES OFFICE

Panasonic Industrial Korea Co., Ltd. [PIKL]
Hanil Group Bldg.11th Fl.,191 Hangangro 2ga,
Youngsans-ku,Seoul 140-702,Korea
Tel: 82-2-795-9600
Fax: 82-2-795-1542

■ PHILIPPINES SALES OFFICE

National Panasonic Sales Philippines [NPP]
102 Laguna Boulevard Laguna Technopark Sta.
Rosa. Laguna 4026 Philippines
Tel: 02-520-3150
Fax: 02-843-2778

© Matsushita Electronics Corporation 2000

080600
Printed in JAPAN